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TSV and Cu-Cu direct bonding: two key technologies for High Density 3D

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1. Introduction

If 3D is not yet an industrial reality, the so called 2.5D, meaning using a piece of silicon as an interposer between plastic board and silicon die, has reach the prototyping phase [1]. True 3D will probably start with a stack of wide I/O Memory attached with a logic circuit, where Through Silicon Vias (TSV) allow for a high bandwidth link between processor and DRAM [2].

In those applications, 3D is used to improve connections between several chips, with only slight modifications of the chips design compared to the 2D version. 3D is also expected to compensate increasing difficulties for Integrated Circuits to go from one node to the following one. Because communication is becoming predominant in today's circuits, wiring improvement (in term of length and capacitance) is a key point. Figure 1 shows an example of reduction of wiring length thanks to the 3D integrationn: in that example, 3D allows a 26% reduction of wire length [3]. To go in that direction, an evolution of current 3D technologies towards higher density interconnects is needed. Two main technologies are concerned by that shrink: flip-chip (interconnect between dice) and TSV. This paper gathers last results obtained by CEA-Leti on reliability and integration with CMOS of direct Cu-Cu bonding and low diameter TSV.

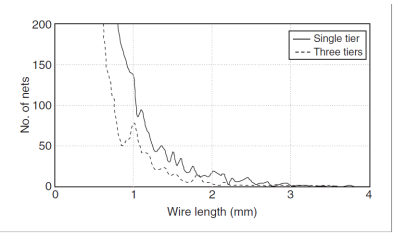

Fig 1. Histogram of wire lengths from a 2D and 3D FFT [1].

2. Technologies description

Integration scheme for High Density 3D

A high density stack implemented by CEA-Leti is presented on Figure 2. The corresponding process flow is compatible with both wafer-to-wafer [4] and chip-to-wafer approach [5].

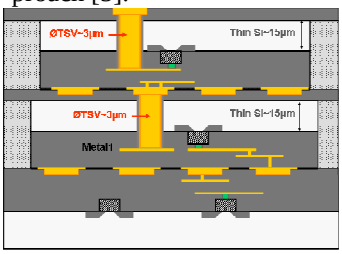

Fig. 2. Integration scheme for High Density 3D Stack

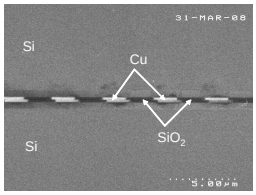

Fig. 3. SEM View of Cu-Cu interconnects.

Direct Cu-Cu bonding, which is the most promising technology for low pitch interconnect, is used for level-to-level interconnect. Cu-filled via-last approach is used for TSV, with a diameter between 1µm and 5µm.

Cu-Cu Bonding

After an optimized damascene-like CMP surface preparation, wafers are bonded at room temperature, atmospheric pressure and ambient air [6]. A post bonding anneal is then applied in order to strengthen the bonding. A thinning of the top silicon wafer (or chips for CTW) down to 15 µm is then carried out. Thanks to Cu-Cu bonding, an interconnect pitch lower than 10 µm has already been demonstrated (Figure 3).

TSV manufacturing

TSV process flow is described on Figure 4. A conformal SACVD TEOS-O3 SiO2 film was used to isolate the TSV. MOCVD TiN was used as a barrier layer against copper diffusion. The copper seeding was achieved by mixing PVD Cu and MOCVD Cu. The TSV were filled with ECD Cu, using specific chemistry and process to obtain voidless filling up to aspect ratio of 10.

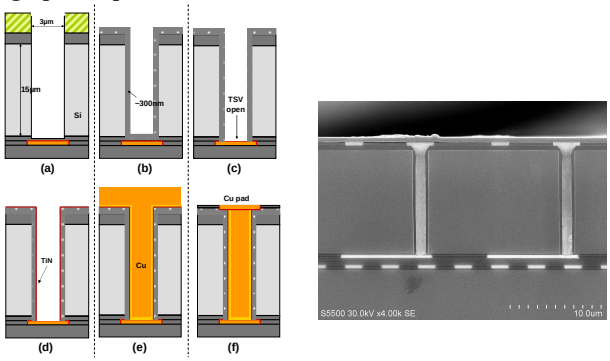

Figure 4 & 5. Process flow and SEM view of TSV. (a) TSV lithography, etching, stripping, (b) isolation with conformal SiO2, (c) via bottom opening with etch-back, (d) TiN barrier deposition, (e) Cu seed deposition and ECD filling, (f) Cu annealing, CMP, followed by a Cu damascene level.

3. Reliability results

Reliability on Cu-Cu bonding

In order to separate TSV and bonding effects, well known simplified TSV were used for test samples. Results of the electrical characterization before cycling [7] demonstrated that the impact of the bonding interface is negligible. A perfect ohmic behaviour was observed on daisy chains.

Figure 6 shows the evolution of resistance for Cu-Cu bonding before and after thermal cycling. No significant degradation was observed. This result points out the good behaviour under thermal stress of interconnect by direct copper bonding process. First results from electromigration tests underlined also that there is no specific degradation at the bonding interface [8].

Reliability on TSV

Thermal Cycling on TSV showed that there is no significant evolution of resistance for small diameter TSV (from 2 µm to 5 µm). Figure 7 shows the drift of resistance for 2 µm diameter TSV chains. Except for 2 bad chips, the drift is negligible. Electromigration tests showed that no voiding occurred in the TSV itself. However, voids at the interface between metal 1 and TSV (Figure 8) were observed and a model has been proposed in reference [9]. This point has to be taken into account for TSV integration.

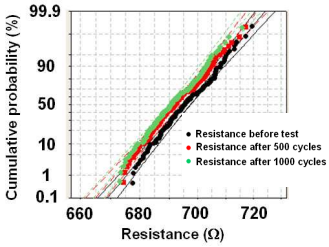

Figure 6: Cumulative probability of Cu-Cu daisy chain resistance before and after 500 and 1000 thermal cycling (-65°C / +150°C)

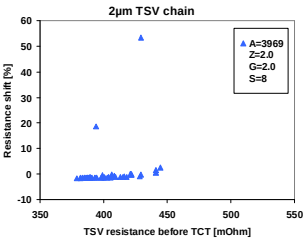

Figure 7. Resistance drift for 4000 TSV chains (2µm diam), after 500 cycles -65/+150°C

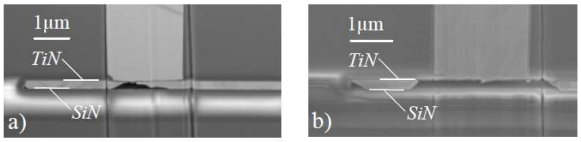

Figure 8. Views of voids under TSV after electromigration.

4. Impact of TSV on CMOS

Integration of 3 µm diameter TSV in a 65nm CMOS has been studied [10].

Thermomechanical impact

Simulation showed that thermo-mechanical impact on transistor is limited, even for a distance between TSV and transistor lower than 2 µm. Figure 9 shows that mobility variation is lower than 5% for a distance greater than 1,8 µm, and no impact is observed beyond 5 µm. Experimental results confirmed that for a logic circuit, we did not see any change of Ion and Ioff depending on the distance from the TSV (fig 10). If we compare to other data published for greater TSV [11], we can think that for a smart integration of TSV in advanced node, small TSV will be required.

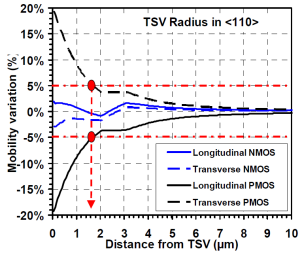

Figure 9: Modeling results of the mobility variation for NMOS and PMOS transistors [10].

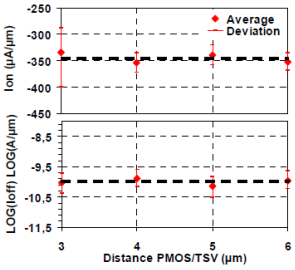

Figure 10: TSV proximity effect on the drain saturation and leakage currents (PMOS) [10].

Electrical Impact

To measure electrical impact of TSV on transistor, a 1.2V square signal was applied to the TSV. Transient measurements performed on a NMOS transistor located 5µm away from the TSV show only 1% variations on the static source current (figure 11), in agreement with the predictive modeling calculations [10], whereas leakage current variation is found to be equal to 1.4µA/µm. These two measurements evidence a capacitive coupling between TSV and MOSFETs. TSV can be seen as a new noise source for circuits, and this has to be taken into account for 3D circuits design, essentially critical circuits like memories or analogic.

Concerning Cu-Cu bonding, contact resistance value (10mohm for 3x3µm² pads) is so small that the IR drop in interconnect can be neglected. To evaluate its impact on the RC delay, this interconnect can be considered as a simple Cu pad, without taking care of the bonding interface.

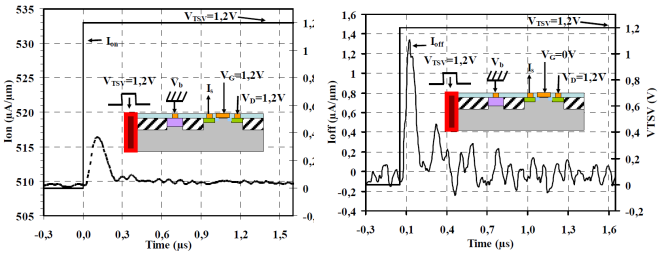

Figure11: Experimental measurement of TSV dynamic coupling effect on drain saturation current (left) and leakage current (right) of NMOS transistors (TSV/NMOS transistors distance =5µm).

5. Conclusion

In order to address high density 3D integration, CEA-Leti is developing low pitch interconnect with Cu-Cu bonding and low diameter TSV. For both technologies, it has been demonstrated that thermal cycling has no significant impact on resistance value. Electromigration results are also promising, even if a specific care must be taken for TSV-Metal 1 connection. Thanks to those reliability results, we can be confident that integration of those technologies will have no impact on reliability at the system level.

Thanks to simulation and experiments, it has also been outlined that impact of TSV on CMOS is limited beyond 2 µm distance. An electrical coupling between TSV and transistor has been demonstrated, and will be taken into account to define design rules of high density 3D circuits.

Acknowledgement

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