Performance Evaluation of a Logic-IP Compatible (LIC) Embedded DRAM with Cylinder Capacitors in Low-k/Cu BEOL Layers

LSI Research Laboratory / *Production and Technology Unit, Renesas Electronics Corporation  
1120 Shimokuzawa, Chuou-ku, Sagamihara, Kanagawa 252-5298, Japan  
Phone: +81-42-771-0689  Fax: +81-42-771-0692  e-mail: ippei.kume.xz@renesas.com

Introduction

Embedded DRAMs (eDRAMs) are attractive for realizing high bandwidth, low latency, and low power of the memory-logic interface with small cell size [1-2]. In the conventional “capacitor over bit-line (COB)” structure, cylinder capacitors for storage nodes are located between M1 and bit-lines, and bypass-contacts need to be added to the conventional contacts for connecting CMOS transistors to M1 (Fig.1). For deep scaling beyond 40 nm technology, higher cylinder capacitors are needed to keep the node capacitance (Cs) per each cell. This may lead to significant increase of the contacts (CT) height, parasitic resistance and capacitance, or even RC-delay of the logic parts in the eDRAM circuit.

We have proposed a novel concept of the logic-IP compatible (LIC) eDRAM containing cylinder capacitors in low-k/Cu BEOL layers, and confirmed feasibility of the capacitor integration with low CT heights to keep compatibility with standard CMOS logic IPs [3]. The LIC-eDRAM is categorized as a “BEOL memory,” of which memory elements are located in interconnect layers such as MRAM [4] and ReRAM [5].

In this paper, we focus on the logic delays of the LIC-eDRAM referred to those of the pure CMOS logics obtained by the circuit simulation for 28nm-node in conjunction with the actual measurement for 40nm-node test-chips.

Circuit simulation for 28 nm node eDRAM

Simulation was conducted by using a motif circuit of ring oscillator with an inverter chain designed for 28 nm-node (Fig.2). Here, we are focusing on the contact resistance and capacitance as simulation parameters, which are functions of the normalized contact height, “X”, referred to that in a 28nm-node pure logic LSI. The parasitic capacitances at the input and output terminals were extracted based on their layouts and vertical structures of the inverters (Fig.3).

The parasitic capacitance of the inverters in the eDRAM, ΔC, enlarged with increasing X as well as the number of CT to each diffusion layer (Fig. 4).  Fig. 5 plots the normalized gate-delays (Δτg) as a function of the CT height, or essentially ΔC. Here, we changed the CT resistance (Rct) normalized to that in the pure logic LSI (Rct: x=1.5~3.0). Δτg increases with the CT height (X), or essentially ΔC, and higher Rct also raises Δτg. Suppression of the contact height and resistance enables us to realize LIC-eDRAMs, within Δτg=5%, even for 28nm-node and beyond.

Performance of 40nm-node LIC-eDRAM

Performance of the 40 nm-node LIC-eDRAM device with 7-layer low-k/Cu BEOL is demonstrated. Ring oscillator with an inverter chain was measured as an indicator of the logic performance, and the retention characteristics of the 512 kb proto-type DRAM macro was evaluated (Table I).

The LIC-eDRAM embeds cylinder capacitors in the M1-M2 layers, which meet the target capacitance Cs=13fF/cell (Fig. 6). As the double-stacked CTs connected M1 to the S/D diffusion areas and the poly-gate electrodes through the bit-line layer, the CT resistances were suppressed below 2-folds to those in the pure logic parts. Integrated cylinder capacitors with thin dielectric of ZrO2 were confirmed to guarantee 10-year TDDB lifetime at 105°C under the constant bias of half Vcc (0.6 V) (Fig.7). Meanwhile, the LIC structure and its fabrication process gave no impact on the static characteristics of the logic CMOS transistors (Fig. 8). Little degradation of inverter delay, Δτg~5 %, in the LIC-eDRAM supports compatibility to the standard CMOS logic IPs (Fig. 9). The DRAM macro operation was also confirmed on the 40nm-node LIC-eDRAM test-chips, and the retention time was found to be in the range of milliseconds (Fig.10).

Conclusion

Feasibility of the LIC-eDRAM with cylinder capacitors embedded in the low-k/Cu BEOL layers was demonstrated. Reduction in the contact height is crucial to minimize the logic delay especially beyond 28 nm-node eDRAM to keep the logic IP compatibility. The BEOL memory structure added on standard CMOS devices is suitable for widening eDRAM applications combined with a variety of leading-edge standard CMOS logic IPs.

References

Fig. 1 Schematic cross-sectional images of various LSI structures. “Logic-IP compatible (LIC)” concept features “capacitor in porous low-k (CAPE)” to reduce parasitic components due to the additional contact stack\[3\]. This concept is a key to utilize the same logic IP in the eDRAM.

Table I TEG structures and measurement conditions for logic and DRAM performances, based on 40nm-technology.

<table>
<thead>
<tr>
<th>TEG Structure</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>- 199-stage ring oscillator</td>
<td>- $V_i = V_i = 1.1 \text{V} / 25^\circ\text{C}$</td>
</tr>
<tr>
<td>- Inverter with F/O=1</td>
<td>- $V_{ai} = 1.25 \text{V} / 105^\circ\text{C}$</td>
</tr>
<tr>
<td>- 2 contacts for each diff.</td>
<td>- $V_{ai} = 1.25 \text{V} / 105^\circ\text{C}$</td>
</tr>
</tbody>
</table>

Fig. 2 Simple circuit model to estimate the gate delay in the eDRAM structures. An inverter chain includes CMOS transistors, contacts, and metal-1 interconnects. All simulation was performed onto the 28nm-node assumption in this work.

Fig. 3 Extraction procedure of input/output parasitic capacitance in inverters to estimate gate delay. Vertical structure and layout are inputted to the simulator to calculate $\Delta C$.

Fig. 4 Increase in parasitic capacitance, $\Delta C$, of the eDRAM structures as a function of contact height, which is normalized with that of the pure-logic.

Fig. 5 Simulation results of increase in inverter delay as a function of normalized contact height. Degradation is assumed to be independent of contact-height and is varied as a parameter in this plot.

Fig. 6 Cross-sectional TEM images of the LIC-eDRAM integrated into the 40nm-CMOS, in which the capacitors were embedded in M1-M2 layer. *MPS-SiOCH: Molecular-pore-stack SiOCH (k~2.55) with sub-nanometer, closed-pore structure [6].

Fig. 7 TDBB reliability of the integrated capacitors in the LIC-eDRAM with 7-level metallization process.

Fig. 8 On-state current of core transistors for the LIC-eDRAM and the pure-logic part. LIC process gave no impact on the static characteristics of the core transistors.

Fig. 9 Measured inverter delay of the LIC-eDRAM and pure-logic. Degradation of delay for the LIC-eDRAM is less than 5%.

Fig. 10 Retention characteristics of the eDRAM macros. Milli-second-order retention time DRAM operation is confirmed for the LIC-eDRAM.