1Xnm Copper and Low-k reliability

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1. Introduction

Ensuring the overall reliability of memory and logic chips is critical. In the past decade dielectric and metal reliability of damascene architectures has been extensively studied with numerous dimensional and material scaling scenarios. For logic chips a 1Xnm technology node, such as 11 or 16nm, involves local interconnect half pitch on the order of 11-23nm. For memory these lateral dimensions are below 20nm with a higher wire aspect ratio when compared to logic. From a material perspective the typical choice of dielectric is SiO$_2$ or air gap for a large class of memories. For high performance applications, scaling the insulator k-value towards 2.0 becomes imperative despite of the fact that the mechanical properties of these low-k materials are weak. Reliability mechanisms and models need to be refined, new materials introduced, processes improved in order to meet the reliability requirements at 1Xnm.

2. Dielectric reliability

Characterizing intrinsic leakage and breakdown properties of thin low-k materials is enabled by planar capacitors [1]. Fig. 1 shows breakdown field measurements for a wide range of materials. Below a k-value of 2.5 it becomes increasingly difficult to ensure high breakdown field, which is reflected by the scatter of the experimental data below k=2.5. Early breakdown can be induced by porogen residues (sp$_2$ carbon), which in turn induces high leakage current. On the other hand the trend determined by the dotted line also evidences that obtaining 7 MV/cm at k=2.0 is viable. The overall decreasing trend in the electric field strength can be explained by internal porosity induced field enhancement [2]. The intrinsic breakdown decreases when k decreases, hence the maximum electric field ($E_{\text{max}}$) at which 10years user lifetime can be obtained decreases.

From time dependent dielectric breakdown (TDDDB) measurements on k=3.2, 3.0, 2.5 and 2.0 dielectrics, $E_{\text{max}}$=3.08, 2.85, 2.7 and 2.05MV/cm was obtained, respectively. These data show that even at k=2.0 the intrinsic TDDDB lifetime is above 10 years. However, not only the k-value, but the dielectric thickness needs to scale as well. On one hand the half pitch is expected to fall below 20nm, on the other hand in a dual damascene architecture via misalignment causes reduced spacing. When the dielectric thickness is decreased below 20nm it is accompanied by further lifetime reduction and the breakdown distributions are characterized by decreased Weibull slopes. For example, when the dielectric thickness is reduced from 60nm to 20nm the measured Weibull slope decreases from around 4 to values close to 1. In the past years several TDDDB lifetime models (E-model, root-E, power-law, etc.) were put forward, which were mainly based on damascene architectures [3-7]. In Fig. 2 time dependent dielectric breakdown measurements conducted on planar structures are summarized. This planar setup enables the investigation of dielectric only properties without any influence from damascene processing. The long term reliability data strongly suggest power law dependence for describing voltage acceleration [8]. Although power law acceleration is less conservative than E or root-E models, it is important to point out that at low percentile the difference between acceleration models can be less dominant than the breakdown statistics itself. Besides the intrinsic dielectric properties various mechanisms linked to damascene etch, ash, clean, barrier deposition, CMP, cap layer plasma treatments, layout, etch stop layers in the stack, line edge roughness, double patterning techniques and the integration approach are known to influence damascene TDDDB.

![Fig. 1 Breakdown field as function of k-value for 60nm dielectric thickness at 100°C](image)

![Fig. 2 TDDDB measurements over a wide range of electric fields. The data suggest power law dependence.](image)
In future scaling scenarios the relative importance of these effects increases. For example, line edge roughness leads to unwanted local field enhancement, which in turn causes early breakdown [9]. The relative importance of correlated and un-correlated line edges are plotted in Fig. 3. When analyzing the model presented in [9] it appears that besides line edge roughness the tapering of the wires, due to field enhancement close to the top interface, can have a significant influence as well.

Fig. 3 Impact of uncorrelated (ρ=0), half correlated (ρ=0.5) and correlated (ρ=1) line edges on TDDB lifetime. θ is the tapering angle.

3. Metal reliability

Nowadays, the conductor choice for most interconnects is copper. When the wire dimension is scaled below 20nm the metal resistivity significantly increases, which is also known as the size effect (Fig. 4). On one hand wire resistance increase is detrimental for performance. On the other hand for a given material system the copper reliability decreases with each new technology generation, because the interconnect lifetime is approximately proportional to the product of the width and height and the relative importance of interfaces increases when the dimensions are reduced. Fig. 5 shows the measured lifetime as a function line width. A conventional Ta-based metal barrier is used along with an SiC(N) copper cap. As the line width scales below 30nm, the electromigration (EM) reliability significantly decreases. For example, at 20nm critical dimension J\text{max}=2.2 \text{ MA/cm}^2 can be calculated for SiO\text{}2, while for low-k a significantly lower value of J\text{max}=0.8 \text{ MA/cm}^2 is obtained.

Fig. 4 Resistivity of copper lines for 75nm tall interconnects

Further scaling requires significant EM improvement both for SiO\text{}2 and low-k interconnects. Alloying copper with Al or Mn, using self aligned CuSiN, CuGeN, MnSiO were all shown to improve EM lifetime, because of lowered grain boundary or copper/cap diffusion rates. A most significant lifetime enhancement is obtained when metal cap layers are implemented [8-13]. At 55nm line width a 100X median lifetime improvement is reported for CoWP. Although the median lifetime significantly improves, typical failure distribution widths are 0.3 for processes with dielectric cap and on the order of 0.9 for CoWP caps. Therefore, at lower percentile failure rates (e.g. 100ppm; t0.01%) the advantage of using a metal cap is reduced to 10X only; albeit still significant. Further line-width reduction may call for alternatives beyond metal caps such as copper replacements without EM issue. Although other metals were already investigated, at 1Xnm copper is unlikely to be replaced, because of its lower resistance as compared to other metals. Below 10nm eventually copper will need to be replaced.

5. Summary

Dielectric and metal reliability aspects were sketched from scaling perspective to 1Xnm.

References