Through Silicon Via (TSV) Fabrication with Low-κ Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current

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ABSTRACT
Through silicon via (TSV) with acceptable sidewall roughness is achieved with careful process optimization. To benefit the performances of 3D IC, TSV must introduce small electrical parasitic such as capacitance. Low-κ liner with conformal step coverage is successfully integrated in TSV structure to reduce the parasitic capacitance by ~28% compared with conventional PE-TEOS liner at the expense of higher leakage current.

Key words: TSV, liner, capacitance, low-κ

INTRODUCTION
Through silicon via (TSV) has emerged as an essential enabler for the next generation of integrated circuits and systems for continuous performance growth (“More Moore”) and functional diversification (“More than Moore”). TSV is commonly fabricated by high aspect ratio deep silicon etching, lining with dielectric layer for electrical isolation and super-conformal filling with copper [1] hence forming a metal-oxide-semiconductor (MOS) structure [2] (Fig. 1). Integration of TSV poses new challenges such as mechanical stress [3] and electrical parasitic [4]. TSV differs from conventional planar interconnects that are embedded in the dielectric in terms of its electrical coupling with the doped Si substrate through the MOS structure. TSV parasitic capacitance has the most predominant impact on the circuit operation [4]. It is therefore imperative to reduce the TSV capacitance. Low-κ dielectric can enable significant reductions in the CMOS backend interconnect capacitance and offers many advantages in circuit performance [5]. In this work, low-κ dielectric is successfully integrated in TSV as a liner. The implications on TSV capacitance and leakage current are discussed.

EXPERIMENTAL
TSV (φ = 5μm) with aspect ratio of 1:2 are fabricated on 8” p-Si wafer. This aspect ratio is chosen for ease of fabrication and is sufficient to study the electrical properties of the liner. The TSV is etched by using a BOSCH process in a deep reactive ion etcher (DRIE) using oxide hard mask. The liner is deposited in a plasma-enhanced CVD chamber at temperature 400°C using TEOS and Black Diamond precursors for oxide and low-κ liner respectively. Subsequently Ta barrier and Cu seed are sputtered followed by super-conformal Cu ECP filling. The Cu overburden is then removed by CMP. Contact holes are opened on oxide layer and Al is deposited and patterned to form contact pads for electrical probing.

RESULTS AND DISCUSSION
Structure Fabrication
In order to achieve a robust TSV, sidewall roughness (from scallop) and oxide hard-mask undercut must be kept as small as possible to ensure void-free and conformal Cu filling. Table I is a summary of TSV etching results using three recipes. When a single mask is used for hard-mask and Si etching, the addition of a small quantity of C4F8 during etching cycle improves both roughness and undercut (Process A vs. B).

In Fig. 2, TSV with PE-TEOS liner as well as low-κ liner are fabricated with conformal step coverage. No void or delamination is observed in the Cu core after filling.

Electrical Measurement
Simulated CV characteristics of MOS structure at high frequency as a function of dielectric constant (κ) is shown in Fig. 3. In principle, the capacitance value of TSV can be lowered by using liner with smaller κ value. Fig. 4 shows the measured CV curves at 100 kHz for both PE-TEOS liner and low-κ liner at an average thickness of ~205nm. The capacitance changes from accumulation to inversion region as the bias voltage increases demonstrating a typical p-Si behaviour. The effective dielectric constant of the low-κ material is estimated to be ~2.8. The capacitance value is lowered by ~28% by replacing PE-TEOS liner with low-κ liner. In Fig. 5, CV curve of PE-TEOS liner shows a negative shift in the flat-band voltage (VFB) due to the presence of fixed charge (+Qf). The fixed charge density is estimated to be on the order of ~1.8 x 1012 cm-2. On the other hand, much less fixed charge is induced during deposition of low-κ liner and its VFB is closer to the ideal value.

IV measurement is performed to evaluate the leakage of the dielectric liner. Fig. 6 shows that there is no abrupt breakdown up to at least 3MV/cm for both PE-TEOS and low-κ liner. However, low-κ suffers from much higher leakage current as compared with PE-TEOS liner (Fig. 7). Leakage current resistance is improved by a 350°C annealing in forming gas (N2/H2) for 30min for both liners. Post annealing, the leakage current at mid-distribution is ~ 1.2 x 103 A/cm2 and ~ 6.8 x 104 A/cm2 for PE-TEOS oxide and low-κ liner respectively at an electric field of 2MV/cm. The leakage current value for the PE-TEOS oxide liner is comparable with the value reported in [6]. It is confirmed from CV measurement that the κ value remains at ~2.8 with annealing. Despite its smaller capacitance value, low-κ liner presents much higher leakage current. Therefore, optimization (e.g. thickness, annealing, etc) is required prior to its integration in TSV for 3D IC application. Since low-κ liner has lower elastic modulus than PE-TEOS liner (7.2 GPa vs. 75 GPa), lower thermal stress is induced in the Si substrate (Fig. 8).

CONCLUSION
It is beneficial to keep the TSV parasitic capacitance as low as possible for low latency signal transmission. Low-κ material with κ value of ~2.8 is used as TSV liner and a ~28% reduction in capacitance is obtained. However, the leakage current must be further controlled for 3D IC application.

REFERENCES
Table I  Comparison of TSV etching processes and profiles. When a single masking step is used, the addition of C\textsubscript{4}F\textsubscript{8} during the etch cycle improves the scallop sidewall roughness as well as oxide hard-mask undercut.

<table>
<thead>
<tr>
<th>Process</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask</td>
<td>Single</td>
<td>Single</td>
</tr>
<tr>
<td>Etching Gas</td>
<td>SF\textsubscript{6}, O\textsubscript{2}</td>
<td>C\textsubscript{4}F\textsubscript{8}, SF\textsubscript{6}, O\textsubscript{2}</td>
</tr>
<tr>
<td>Passivation Gas</td>
<td>C\textsubscript{4}F\textsubscript{8}</td>
<td>C\textsubscript{4}F\textsubscript{8}</td>
</tr>
<tr>
<td>Etch Profile</td>
<td>(SEM image of unfilled TSV)</td>
<td>(SEM image of unfilled TSV)</td>
</tr>
<tr>
<td>Roughness (nm)</td>
<td>107-129</td>
<td>68-75</td>
</tr>
<tr>
<td>Undercut (nm)</td>
<td>239</td>
<td>60</td>
</tr>
</tbody>
</table>

Fig. 1  TSV essentially forms an embedded MOS structure in the Si substrate and its parasitic capacitance shows distinct accumulation, depletion and inversion regions depending on gate (Cu core) voltage and frequency. The depletion capacitance ($C_{\text{dep}}$) is a series combination of dielectric capacitance ($C_{\text{ox}}$) and silicon capacitance ($C_{\text{Si}}$).

Fig. 2  Through-silicon via (TSV) having Cu as the core conductor and (a) PE-TEOS liner & (b) low-κ liner shell for electrical isolation. The diameter is ~5 µm and the depth is ~10 µm. Conformal deposition of both dielectric liners is achieved using PECVD.

Fig. 3  Capacitance reduction in MOS structure using low-κ dielectric. (Dielectric thickness is 200nm and the substrate doping, $N_a$, is 1e16 cm\textsuperscript{-3}).

Fig. 4  (a) Plan view of TSV array ($\phi = 5$µm) after CMP removal of the Cu overburden and no sign of Cu debris is found from optical microscope. (b) Electrical MOS structure formed by TSV for probing. The Si substrate is grounded using a p+ contact. The probe pad capacitance is kept low by using thicker oxide below the Al probe pad and formation of TSV array to increase the effective TSV area.

Fig. 5  CV measurement (100 kHz) on TSV structures formed using PE-TEOS oxide liner and low-κ liner. A ~28% reduction in capacitance is obtained by replacing PE-TEOS liner with low-κ liner.

Fig. 6  IV measurement on TSV structure. Low-κ liner is found to suffer from higher leakage current as compared with PE-TEOS oxide liner.

Fig. 7  TSV leakage current at 2MV/cm. Low-κ liner experiences much higher leakage as compared with PE-TEOS oxide liner. The leakage current is reduced after annealing at 350°C for 30min in forming gas for both liners.

Fig. 8  Cu-TSV induces stress in silicon due to thermal mismatch. Since low-κ liner has lower elastic modulus, lower thermal stress is induced in the silicon substrate.