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Simple and Efficient MASTAR Threshold Voltage and Subthreshold Slope Models for Double Gate Structures

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Introduction

Double gate structure is considered as the one of the most promising device to reach the end of the roadmap. Some works proposed threshold voltage model, but they often need numerical solver. The aim of this work is to provide a simple and analytical model for symmetrical double gate device, including quantum and short channel effects. 2D FlexPDE [1] numerical simulations and measurements are performed to validate our model. This model is implemented in MASTAR software, commonly used for the definition of the ITRS roadmap.

Threshold voltage definition

In bulk devices, threshold voltage is defined by gate voltage where the surface potential is equal to $2x\varphi_f$ with φ_f being the Fermi potential. At the contrary, in undoped channel, it has been shown that this definition is incorrect [1, 2]. In this work, we choose to define the threshold voltage by the inflection point on the $C_{gc}(V_g)$ curves, such as:

$$\frac{d^2C_{gc}}{dV_g{}^2} = 0 \quad (1)$$

In the undoped channel case, the depletion charge is negligible, so gate-to-channel capacitance is roughly equal to the derivative of the inversion charge (Q_i) with respect to gate voltage. This threshold definition is equivalent to the maximum of transconductance criterion, in the undoped channel case:

$$\frac{d^2g_m}{dV_g{}^2} = 0 \leftrightarrow \frac{d^3Q_i}{dV_g{}^3} = 0 \leftrightarrow \frac{d^2C_{gc}}{dV_g{}^2} = 0 \quad with \quad I_d \sim \frac{W}{L}\mu Q_i V_d \quad (2)$$

After differentiating (1), it leads to an expression of inversion charge (Q_{ith}), which defines the turn-on condition as:

$$Q_{ith} = \frac{kT}{q}\frac{C_{ox}}{2} \quad (3)$$

Numerical simulations are performed to validate our approach. Fig 2 shows that the threshold voltage extrapolated from inversion charge is indeed equal to gate voltage where dC_{gc}/dV_g is maximum.

Long channel threshold voltage model

To model long channel threshold voltage in a double gate device (fig 1), we write Gauss law in the half of the film:

$$\varepsilon_{si}E_s = qn_i\frac{t_{si}}{2}e^{\left(\frac{q\varphi_s}{kT}\right)} + qN_{ch}\frac{t_{si}}{2} = C_{ox}\left(V_g - V_{fb} - \varphi_s\right) \quad (4)$$

With E_s being the surface electric field, φ_s the surface potential, n_i the intrinsic carrier concentration, N_{ch} the channel doping and t_{si} the film thickness. Using (3), we obtain the expression of the surface electric field at threshold ($\varepsilon_{si}E_s=Q_{ith}$). Replacing in (4), we obtain the surface potential at threshold:

$$\varphi_{s_{th}} = \frac{kT}{q}ln\left(\frac{\frac{kT}{q}C_{ox}+q\,N_{ch}t_{si}}{qn_it_{si}}\right) \quad (5)$$

This leads to the following long channel threshold voltage equation:

$$Vt_{long} = V_{fb} + \frac{2Q_{ith}+qN_{ch}t_{si}}{2C_{ox}} + \varphi_{s_{th}} \quad (6)$$

Fig 3 shows the good agreement of the V_{th} model with numerical simulations for various EOT and t_{si} variation in undoped channel case. Fig 5 shows that our threshold definition is also valid for doped channel ($N_{ch}=10^{18}cm^3$).

Quantum correction for thin devices model

For ultra-thin double gate devices (t_{si}<5nm), quantum effects cannot be neglected. Indeed, carrier distribution near gate oxide has to be corrected. In introducing λ, the dark space quantum length, given by [3, 4], we can easily correct the classical carrier distribution for a double gate device, by using the following equation:

$$n_q(x) = n_0\exp\left(\frac{q\varphi}{kT}\right).\left(1-\exp\left(-\frac{x^2}{\lambda^2}\right)\right).\left(1-\exp\left(-\frac{(x-t_{si})^2}{\lambda^2}\right)\right) \quad (6)$$

Here the first term represents classical carrier distribution and the last two terms quantum correction for respectively top and bottom gates. Integrating (6) and making the ratio between quantum and classical inversion charge, gives a correction factor $CF(t_{si})$. Considering a constant electrical field in the film and equal to $2.Q_{ith}/\varepsilon_{si}$ at threshold (Fig 5), an analytical expression of $CF(t_{si})$ can be obtained based on error function. This is roughly true for thin film, but not for larger one. To ensure the validity of the model, we normalise $CF(t_{si})$ by its value for large t_{si} where quantum correction is negligible (>100nm), its trend is shown on fig 6. After rewriting (4) with the quantum corrected inversion charge expression, we obtain a long threshold surface potential equation, taking into account quantum effects, and so, valid for t_{si}<5nm.

$$\varphi_{s_{thq}} = \frac{kT}{q}\ln\left(\frac{\frac{kT}{q}C_{ox}+q\,N_{ch}t_{si}}{CF_{norm}(t_{si})qn_it_{si}}\right) \quad (8)$$

Replacing (8) in (6), a total analytic expression of long channel threshold voltage, accounting for quantum effects, is obtained. This model has been validated by FlexPDE simulations shown on fig 7.

Short channel effects V_t model using VDT technique

To model short channel effects, we chose to use the Voltage Doping Transformation (VDT) approach [4]. It consists in solving 2D Poisson equation only on virtual cathode in a curvilinear coordinate system. By this way, Poisson equation can be reduced to 1D in introducing an effective channel doping $N_{ch}{}^*$.

$$\frac{d^2\varphi}{dx^2} = q\frac{N_{ch}}{\varepsilon_{si}} - \frac{d^2\varphi}{dy^2} = q\frac{N_{ch}{}^*}{\varepsilon_{si}} \quad (9)$$

Physically it means that the lateral drain-source field influence on the potential barrier height can be replaced by a reduction in doping concentration. $N_{ch}{}^*$ expression is obtained by approximating the potential between source and drain by a parabola:

$$N_{ch}(x)^* = N_{ch} - 2\frac{\varepsilon_{si}}{q}\frac{V_{DS}(x)^*}{L^2} \quad (10)$$

$$V_{DS}(x)^* = V_{DS} + 2(\varphi_d - \varphi(x)) + 2\sqrt{(\varphi_d - \varphi(x))(V_{DS} + \varphi_d - \varphi(x))} \quad (11)$$

where φ_d is the built-in potential, V_{DS} source-to-drain voltage and $\varphi(x)$ the potential along virtual cathode. To avoid iterative calculation, it has been proposed to set $\varphi(x)$ at a constant value [6], $2x\varphi_f$ in case of bulk devices, and to linearize the square root. In the case of double gate device, we choose to set $\varphi(x)=\varphi_{sth}$. It leads to the following expressions of V_t short channel effect (SCE) and DIBL:

$$SCE = 0.75\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{t_{si}}{2}t_{ox}\frac{4\left(\varphi_d - \varphi_{s_{th}}\right)}{L^2} \quad DIBL = 0.75\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{t_{si}}{2}t_{ox}\frac{2\,V_{DS}}{L^2}$$

where 0.75 is a fitting parameter. Subthreshold slope can be obtained from its classical definition [9] and by replacing channel doping by the effective one (10),

$$SS = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{ss}}{C_{ox}} + \frac{1}{C_{ox}}\frac{t_{si}\varepsilon_{si}}{L^2}\left(2 + \sqrt{\frac{\varphi_d - \varphi}{V_{DS}+\varphi_d-\varphi}} + \sqrt{\frac{V_{DS}+\varphi_d-\varphi}{\varphi_d-\varphi}}\right)\right)$$

where C_{ss} is the surface-state capacitance and $\varphi=1.5x\varphi_{sth}$ to guarantee the weak inversion regime. Numerical simulations have been performed to validate $V_t(L)$ for V_{DS}=0.1V (fig. 8,9), DIBL(L) (fig.10,11) and SS(L) (fig.13,14) models for t_{si}=5, 7, 10 nm and EOT=4, 10Å. Moreover, DIBL model is validated by silicon measurement [10] (fig 11, 12). Finally, we proposed in fig. 16 a projection of electrostatics performance for 22nm node typical double gate device.

Conclusion

We described a very simple and fully analytical threshold voltage model for undoped symmetrical double gate devices. The model takes into account quantum effects for ultra thin devices and short channel effects for ultra short devices. EOT, T_{si} and L behavior has been validated by numerical simulation and measurements.

References

[1] www.pdesolutions.com

[2] Q. Chen et al, TED 2003 [3] C, T. Lee et al, TED 1989[4] W. Hänsch et al, SSE 1989 [5] R. Rios et al, IEDM 1994 [6] T. Skotnicki et al, EDL 1988 [7] T. Skotnicki et al, IEDM 1994 [8] R. Gwoziecki et al, TED 1999 [9] S.M.Sze, "Physics of semiconductor devices", J.Wiley and Sons, NY 1981 [10] J-L. Huguenin et al SSDM2010

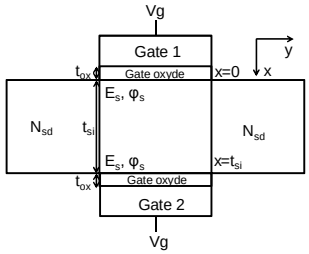

Figure 1: Schematic double gate structure with its main electrical and geometrical parameters.

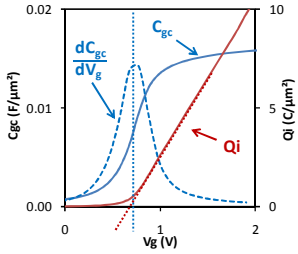

Figure 2: Inversion charge (right axis) and gate to channel capacitance and its derivative (left axis) versus gate voltage generated by FlexPDE.

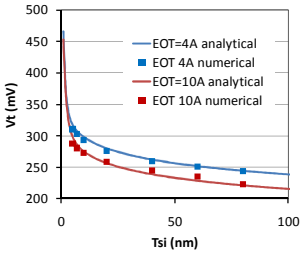

Figure 3: Long threshold voltage variation with t_{si} for EOT= 4 and 10Å.

$$CF(t_{si}) = \frac{Q_{iquantum}}{Q_{iclass}} = \frac{\int_0^{t_{si}} n_0 \left(\exp\left(\frac{-qFx}{kT}\right) + \exp\left(-\frac{qF(t_{si}-x)}{kT}\right)\right).\left(1-\exp\left(-\frac{x^2}{\lambda^2}\right)\right).\left(1-\exp\left(-\frac{(x-t_{si})^2}{\lambda^2}\right)\right)dx}{\int_0^{t_{si}} n_0 \left(\exp\left(\frac{-qFx}{kT}\right) + \exp\left(-\frac{qF(t_{si}-x)}{kT}\right)\right)dx} \quad where \quad F = \frac{Q_{ith}}{\varepsilon_{si}}$$

Figure 4: Quantum correction factor expression before normalization.

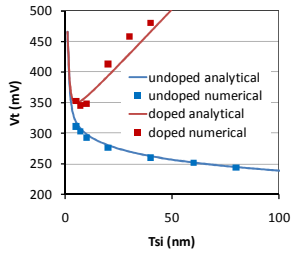

Figure 5: Long threshold voltage variation with tsi for EOT= 4 Å and N_{CH}=1e15 and 1e18 cm^{3}.

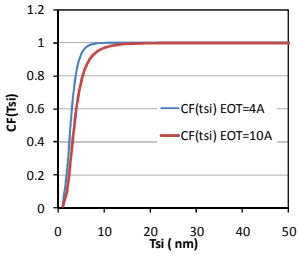

Figure 6 Correction factor trend versus t_{si} for EOT= 4 and 10Å.

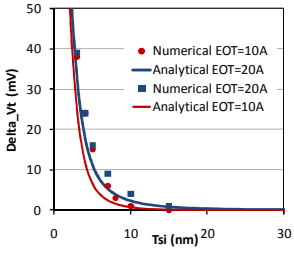

Figure 7: Delta Vt between classical Vt and Vt quantum corrected versus t_{si} for EOT= 4 and 10Å.

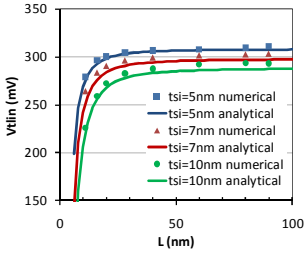

Figure 8: Threshold voltage for V_{DS}=0.1V versus L for EOT=4Å.

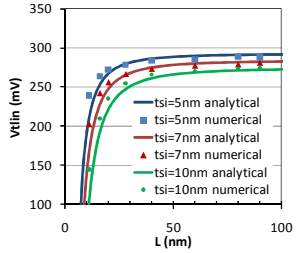

Figure 9: Threshold voltage for V_{DS}=0.1V versus gate length for EOT=10Å.

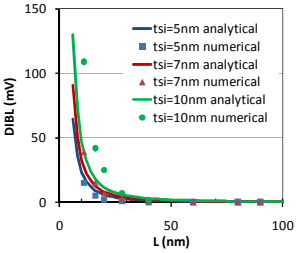

Figure 10: DIBL for V_{DS}=0.7V versus gate length for EOT=4Å.

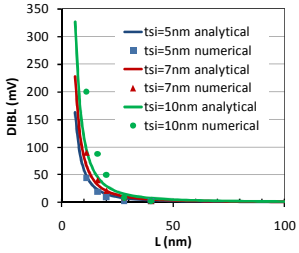

Figure 11 DIBL for V_{DS}=0.7V versus gate length for EOT=10Å.

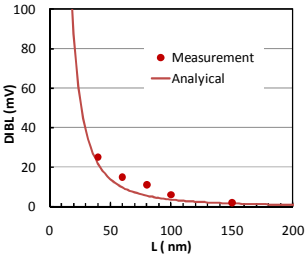

Figure 12: DIBL for V_{DS}=1V versus gate length for EOT=22Å and t_{si}=8nm.

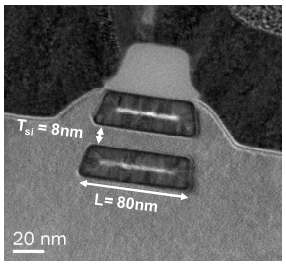

Figure 13: TEM cross section of characterized double gate device.

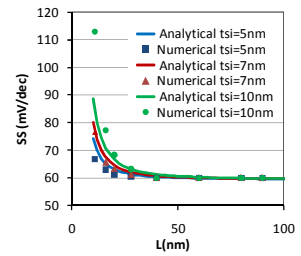

Figure 14: Subthreshold slope for V_{DS}=0.1V versus gate length for EOT=4Å and t_{si}=5, 7 and 10nm.

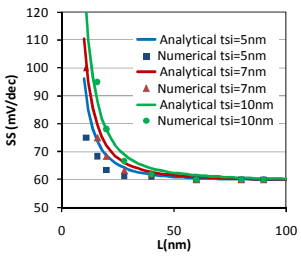

Figure 15: Subthreshold slope for V_{DS}=0.1V versus gate length for EOT=10Å and t_{si}=5, 7 and 10nm.

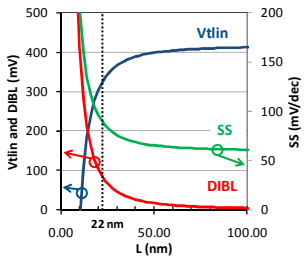

Figure 16: Projection of 22nm node electrostatics performance, t_{si}=15nm, EOT=9.5Å and Vdd=0.9V.