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Accurate and Ready-to-use Parasitic Capacitances Models for Advanced 2D/3D CMOS Device Structure Comparison

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Introduction

Parasitic capacitances become a performance constraint for ultra-scaled technologies. In this work we present a unified solution to quickly evaluate capacitances on Bulk-Si, FDSOI, planar double gate (DG) [4] and FinFET [5] devices. Our model is accurate, ready-to-use for architecture comparison and easily adaptable for other structures such as QW transistors. In contrast to previous works on planar devices [1-3], gate-to-contact capacitance and corner capacitance are accurately modeled, quantum effects are taken into account thanks tabulated data, and inner fringe capacitance screening is physically implemented. Concerning FinFET, every parasitic components have been modeled. Finally, all models, including FINFET, have been validated by 2-3D numerical simulations and were used to evaluate parasitics impact following ITRS-roadmap requirement.

Parasitic capacitances modeling on planar architecture

In order to model capacitances for planar architecture (Fig 1), we use the classical parallel plate equations for C_{gc}, C_{ov}, C_{pcca} and conformal mapping approach [6] for C_{of}, C_{if}, $C_{pccatop}$ (capacitance between top of the gate and contact) and C_{corner} (capacitance due to gate extension on STI) evaluation, which are composed of elliptical electric field lines. Conformal mapping consists in transforming the initial cartesian coordinate system (x,y) in an elliptical one (x',y') by applying the transformation function given in [7]:

$$F(x+jy)=(x'+jy') \quad \text{where} \quad F=\arccos$$

After some mathematical operation fringe capacitance C_1 per unit of width can be calculated as a plate one in the new coordinate system, where (x_1,x_2,y_1,y_2) are described on fig 2 :

$$C_1 = 2\frac{\varepsilon}{\pi}\left[\sinh^{-1}\left(\sqrt{\frac{\sqrt{x_1^2+\min(y_2,x_2)^2+2.x_1\min(y_2,x_2)^2}}{\sqrt{|x_1^2-y_1^2|}}}\right)-\sinh^{-1}\left(\sqrt{\frac{x_1}{\sqrt{|x_1^2-y_1^2|}}}\right)\right]$$

To model capacitance in the region for $x<x_1$ and $y<y_1$, we use the following equation, given by [4]:

$$C_2=0.35\frac{\varepsilon_{ox}W}{2\pi}\ln\left(\frac{\pi W}{\sqrt{|x_1^2-y_1^2|}}\right), \quad \text{with W: device width}$$

Consequently, the total fringe capacitance is calculated by $C=W.C_1+C_2$, after properly replacing (x_1,x_2,y_1,y_2). Knowing oxide thickness (t_{ox}), gate length (L), device width (W), gate-to-contact distance (considered here as spacer thickness (t_{sp})), and gate height (H_g), all fringe capacitances can be calculated (in bulk for C_{of}, we have to set $(x_1,x_2,y_1,y_2)=(t_{ox},H_g,0,t_{sp})$). To validate this model, 2D numerical simulations have been performed with FlexPDE [8] software. From extracted potential maps we remark that flat component of C_{pcca} has to be corrected in subtracting from gate height the distance where iso-potential surface are elliptical. We estimate this dimension to be the half of the gate-to-contact distance (fig 3). After this correction model gives a good agreement with numerical simulation (fig. 4, 5).

To model C_{corner}, conformal mapping has to be adapted for each component because of their 3D nature (fig.6). For the $C_{cornerSD}$ component, we divided the gate extension in n slices and applied conformal mapping on each, after that we sum the n elementary capacitances. We repeat this operation for $C_{cornercontact}$ and $C_{cornercontacttop}$. $C_{cornerG}$ can be modelled with classical conformal mapping. 3D simulation has been performed with Raphael software [9] to validate the model (Fig 7, 8). Top of table 1 summarizes equations to evaluate parasitic on bulk devices, which can easily be adapted to FDSOI and planar DG.

Parasitic capacitances modeling on 3D architecture

To evaluate parasitic capacitances on a FINFET device (fig 1 bottom), we use the same methodology as in the planar case. Fringe capacitance between the fin and the gate through the spacer $C_{fingate}$ is divided in 4 components (Fig. 1 right), which can be also modeled thanks to conformal mapping by a similar method than for C_{of}. The capacitance between raised S/D and the gate ($C_{gateepi}$) is a parallel plate capacitor and is modeled by the same method than C_{pcca} in the planar case, with the similar correction explained on fig 3. Then C_{gc}, C_{ov}, C_{if}, C_{pcca} and C_{corner} are evaluated as in the planar case. All equations are summarized at the bottom of table 1. The model is validated by 3D simulations done with Raphael software (fig. 9, 10).

Parasitics Evaluation in the ITRS Roadmap

Following ITRS roadmap projection [10], we evaluate capacitances for Bulk, FDSOI, planar DG and FinFET until 2021 in the Low Standby Power case. From gate length (L), contacted poly pitch (CPP), film or junction thickness (T_{si} or X_j) and EOT, we estimate all dimensions for all devices: width (W) is assumed to be 3xCPP, spacer thickness (t_{sp}) to (CPP-L)/3, gate height (H_g) to 2xL, gate extension (W_{ext}) to L and overlap to L/4. For FinFET, specific dimensions are needed: fin height (H_{si}) is assumed to be $3xT_{si}$, hard mask thickness (T_{mask}) is equal to T_{si}, fin pitch (FP) to (H_{si} + T_{si}) and N_{fin} to W/FP. Figure 11 shows the comparison of total capacitance ($C_{par}+C_{gc}$, where $C_{par}= C_{ov}+C_{of}+C_{if}+C_{pcca}+C_{corner}$) normalized by C_{gc} between ITRS data and our evaluation. We can see that parasitics weight and their evolution with scaling are under-estimated by the current ITRS methodology. In addition, we compared planar DG to FinFETs in term of parasitics and found that planar DG presents a better C_{tot}/C_{gc} ratio. Since their electrostatic will be similar, planar DG seems to be a competitive solution to reach best performance to the end of roadmap.

Toward circuit benchmarking

To perform more sophisticated circuit performance assessment, capacitances have to be modeled with their voltage dependency. Junction capacitance is evaluated with the classical equation, given in [1]. For gate capacitance, we use a tabulated model [11]. Charge-Potential Q(ψ) data are generated thanks UTOX [12] for all architectures and C(V) curves are re-built from this data. So we guarantee the accuracy of a Poisson Schrödinger solver and the rapidity of an analytical model. This approach has been validated by silicon measurements (Fig 12). In a first approximation, inner-fringing capacitance has been considered constant. But in reality, as mentioned in previous work [3] C_{if} is roughly negligible in accumulation and inversion regime due to screening (because source and drain are connected) and reach its maximum in depletion regime. To model the screening, we use the method describe by Fleury et al. [13].

$$C_{if}(V_g)=\frac{C_{ifmax}C_{ox}^2}{(C_{ox}+C_{gc}(V_g)-C_{min})^2+C_{ifmax}(C_{gc}(V_g)-C_{min})}$$

Fig. 13 shows the good agreement of analytical model and numerical simulation done with FlexPDE.

Conclusion

In this paper, we present accurate and easily implementable capacitance models for the evaluation of parasitics in advanced CMOS technologies such as scaled Bulk, FDSOI, FinFET and Planar Double Gate. In addition, compatibility with circuit simulator is ensured by using continuous CV curves and the screening of the inner fringe capacitance.

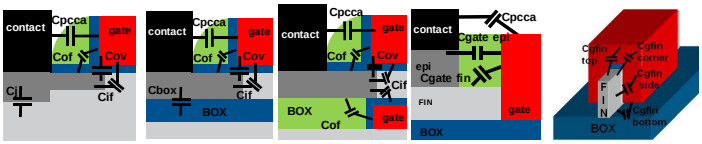

Figure 1: Schematic cross section of studied devices and their parasitic capacitances: from left to right: bulk, FDSOI, planar DG and FINFET.

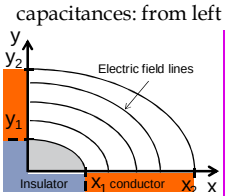

Figure 2: Conformal mapping coordinate system.

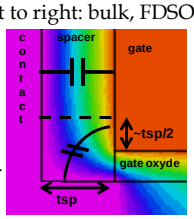

Figure 3: Potential map generated by FlexPDE

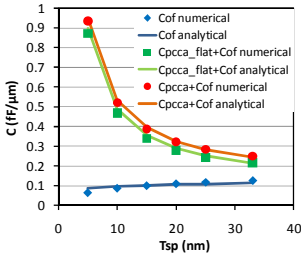

Figure 4: Parasitic capacitances for planar architecture for t_{sp} variation with t_{ox}=2nm and H_g=80nm.

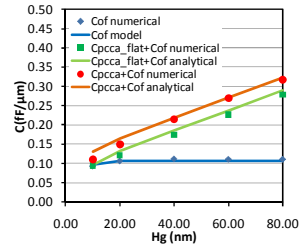

Figure 5: Parasitic capacitances for planar architecture for H_g variation with t_{ox}=2nm and t_{sp}=20nm.

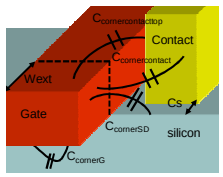

Figure 6: C_{corner} components

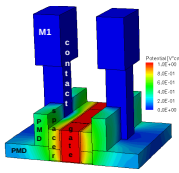

Figure 7: C_{corner} 3D simulation kit.

W_{ext}=70nm C_s = 30 nm	Analytical C_{corner} (F)	Numerical C_{corner} (F)
L=46nm	1.30e-17	1.37e-17
L=406nm	5.21e-17	5.21e-17
L=790nm	8.63e-17	9.66e-17

Figure 8: C_{corner} model validation by 3D simulation for various L.

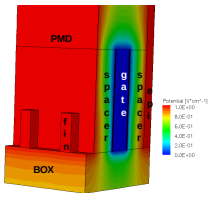

Figure 9: FINFET 3D-simulation kit

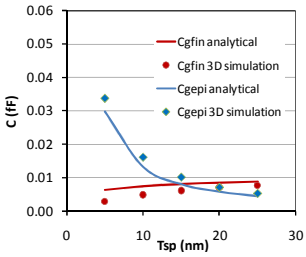

Figure 10: Parasitic capacitances for FINFET architecture for spacer thickness variation with t_{ox}=2nm, H_g=80nm, T_{si}=10nm, H_{si}=30nm.

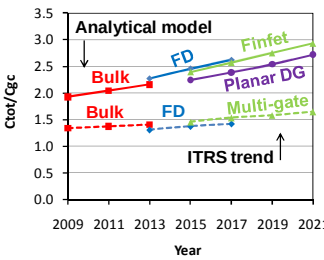

Figure 11: C_{tot}/C_{gc} versus year for ITRS data and our evaluation.

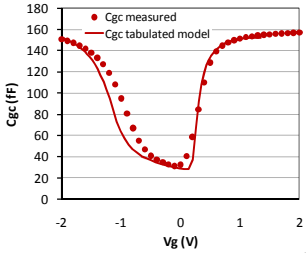

Figure 12: Gate capacitance model validation with a long (L=10µm) C45 bulk device measurement.

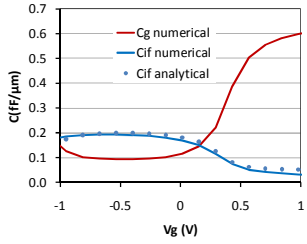

Figure 13: Inner fringe capacitance versus gate voltage for a bulk device.

Planar capacitances equations:

$$C_{of}=\frac{2}{\pi} W\varepsilon_{spacer}\sinh^{-1}\left(\sqrt{\frac{\min_{of}^2+2\,t_{ox}\min_{of}}{t_{ox}}}\right)+0.35\,\varepsilon_{spacer}\frac{W}{\pi}\ln\left(\pi\frac{W}{t_{ox}}\right)\ ,\ \text{where } \min_{of}=\min(H_g,t_{sp})$$

$$C_{ifmax}=\frac{2}{\pi} W\,\varepsilon_{si}\sinh^{-1}\left(\sqrt{\frac{\min_{if}^2+2\,t_{ox}\min_{if}}{t_{ox}}}\right)+0.35\,\varepsilon_{si}\frac{W}{\pi}\ln\left(\pi\frac{W}{t_{ox}}\right)\ ,\ \text{where } \min_{if}=\min\left(\frac{L}{2},Xj\right)$$

$$C_{pcca}=C_{pcca_{flat}}+C_{pcca_{top}} \qquad C_{pcca_{flat}}=N\,Lc\left(tp-\frac{\min_{of}}{2}\right)\frac{\varepsilon_{spacer}}{t_{sp}}$$

$$C_{pcca_{top}}=\frac{2}{\pi} W\,tp\,\varepsilon_{pmd}\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{sp}^2+\left(\frac{L}{2}\right)^2}+t_{sp}L}{t_{sp}}}\right)+0.35.\varepsilon_{pmd}\frac{N\,Lc}{\pi}\ln\left(\pi\frac{\frac{L}{2}}{t_{sp}}\right)$$

$$C_{corner}=C_{corner_{SD}}+C_{corner_G}+C_{corner_{sidewall_{contact}}}+C_{corner_{topgate_{contact}}} \qquad C_{cornerG}=C_{corner_{Gbottom}}+C_{corner_{Gfringe}}$$

$$C_{corner_{SD}}=\sum_i\frac{2}{\pi}\frac{i\,H_g}{div}\varepsilon_{spacer}.\sinh^{-1}\left(\sqrt{\frac{\sqrt{\left(\frac{H_g}{div}\right)^2+2\,t_{ox}W_{ext}+W_{ext}^2}}{\sqrt{\left(\frac{H_g}{div}\right)^2-t_{ox}^2}}}\right)$$

$$C_{corner_{Gbottom}}=\frac{2}{\pi} L\,\varepsilon_{STI}\sinh^{-1}\left(\sqrt{\frac{\sqrt{W_{ext}^2+2\,W_{ext}t_{ox}}}{tox}}\right)+0.35.\varepsilon_{STI}\frac{W}{\pi}\ln\left(\pi\frac{W}{t_{ox}}\right)$$

$$C_{corner_{G_{fringe}}}=\sum_i 2\frac{2}{\pi}\frac{i\,L}{2\,div}\varepsilon_{STI}\ \sinh^{-1}\left(\sqrt{\frac{\sqrt{\left(i\frac{L}{2\,div}\right)^2+2\,t_{ox}W_{ext}+W_{ext}^2}}{\sqrt{\left(i\frac{L}{2\,div}\right)^2-t_{ox}^2}}}\right)$$

$$C_{corner_{contact}}=\frac{2}{\pi}\,tp\,\varepsilon_{spacer}\left(\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{sp}^2+2\,(C_s+W_{ext})\,C_s+(C_s+W_{ext})^2}}{\sqrt{t_{sp}^2-C_s^2}}}\right)-\sinh^{-1}\left(\sqrt{\frac{t_{sp}^2}{t_{sp}^2-C_s^2}}\right)\right)$$

$$C_{corner_{contacttop}}=\sum_i 2\frac{2}{\pi}\frac{i\,W_{ext}}{div}\varepsilon_{spacer}\ \sinh^{-1}\left(\sqrt{\frac{\sqrt{Hmax_{eff}^2+2\,Hmax_{eff}\,Hmin_{eff}}}{Hmin_{eff}}}\right)$$

$$Hmin_{eff}(i)=\sqrt{(Cs+i\,Wext/div)^2+t_{sp}^2}\ \text{ and }\ Hmax_{eff}(i)=\sqrt{(Cs+i\,Wext/div)^2+(t_{sp}+L)^2}-Hmin_{eff}(i)$$

FINFET capacitances equations:

$$C_g=2\,H_{si}N_{fin}\frac{(L_g-2L_{ov})\varepsilon_{ox}}{t_{ox}} \qquad C_{ov}=2\,H_{si}N_{fin}\,L_{ov}\frac{\varepsilon_{ox}}{t_{ox}}+N_{fin}T_{si}L_g\frac{\varepsilon_{ox}}{t_{mask}}$$

$$C_{ifmax}=2\frac{2}{\pi}N_{fin}H_{si}\varepsilon_{si}\sinh^{-1}\left(\sqrt{\frac{\sqrt{\left(\frac{T_{si}}{2}\right)^2+2\,t_{ox}\frac{T_{si}}{2}}}{t_{ox}}}\right)+2\,N_{fin}0.35\,\varepsilon_{si}\frac{H_{si}}{\pi}\ln\left(\pi\frac{H_{si}}{t_{ox}}\right)$$

$$C_{gate_{epi_{betweenfin}}}=\frac{N_{fin}(H_{si}+H_{epi})(FP-T_{si}-2\,t_{ox}-t_{min})\varepsilon_{spacer}}{t_{sp}};\quad t_{min}=\min\left(t_{sp},\frac{FP-T_{si}}{2}-t_{ox}\right)$$

$$C_{gate_{epi_{onfin}}}=N_{fin}T_{si}(H_{epi}-t_{mask}-t_{min}/2)\frac{\varepsilon_{spacer}}{t_{sp}}\ ;\ t_{min}=\min(t_{sp},H_{epi}-t_{mask})$$

$$H_{epi}<t_{mask}\Longrightarrow C_{gate_{epi_{onfin}}}=0 \qquad C_{gate_{epi}}=C_{gate_{epi_{betweenfin}}}+C_{gate_{epi_{finedge}}}+C_{gate_{epi_{onfin}}}$$

$$C_{gate_{contact_{flat}}}=\frac{W_{footprint}\left(H_g-H_{epi}+t_{mask}-\frac{t_{min}}{2}\right)\varepsilon_{spacer}}{t_{sp}}\ ;\qquad t_{min}=\min\left(t_{spacer},\frac{H_{epi}-t_{mask}}{2}\right)$$

$$C_{gate_{contact_{top}}}=\frac{2}{\pi}W_{footprint}\varepsilon_{pmd}\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{sp}^2+\left(\frac{L}{2}\right)^2}}{\frac{L}{2}}}\right)+0.35\frac{W_{footprint}}{\pi}\varepsilon_{pmd}\ln\left(\pi\frac{\frac{L}{2}}{t_{sp}}\right)$$

$$t_{min_{side}}=\min\left(t_{sp},\frac{FP-T_{si}}{2}\right) \qquad t_{min_{top}}=\min(t_{sp},H_{epi}-t_{mask})$$

$$C_{gfin_{side}}=2\frac{2}{\pi}N_{fin}\,H_{si}\,\varepsilon_{spacer}\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{min_{side}}^2+2t_{min_{side}}t_{ox}}}{t_{ox}}}\right)+2\,N_{fin}0.35\frac{H_{si}}{\pi}\varepsilon_{spacer}\ln\left(\pi\frac{H_{si}}{t_{ox}}\right)$$

$$C_{gfin_{top}}=\frac{2}{\pi}N_{fin}\,T_{si}\,\varepsilon_{spacer}\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{min_{top}}^2+2\,t_{min_{top}}t_{mask}}}{t_{mask}}}\right)+2\,N_{fin}0.35\frac{T_{si}}{\pi}\varepsilon_{spacer}\ln\left(\pi\frac{T_{si}}{t_{mask}}\right)$$

$$C_{gfin_{corner}}=\sum_i 2\,N_{fin}\frac{2}{\pi}\frac{i\,t_{sp}}{div}\varepsilon_{spacer}\ \sinh^{-1}\left(\sqrt{\frac{\sqrt{Hmax_{eff}^2+2\,Hmax_{eff}\,Hmin_{eff}}}{Hmin_{eff}}}\right)$$

$$Hmin_{eff}(i)=\sqrt{(i\,t_{sp}/div)^2+t_{ox}^2} \qquad Hmax_{eff}(i)=\sqrt{(i\,t_{sp}/div)^2+(t_{ox}+T_{si})^2}-Hmin_{eff}(i)$$

$$C_{gfin_{bottom}}=\frac{2}{\pi}2\,N_{fin}\frac{T_{si}}{2}\varepsilon_{box}\sinh^{-1}\left(\sqrt{\frac{\sqrt{t_{sp}^2+2\,t_{sp}t_{ox}}}{t_{ox}}}\right)+2\,N_{fin}0.35\frac{T_{si}}{2\pi}\varepsilon_{spacer}\ln\left(\pi\frac{T_{si}}{2\,t_{ox}}\right)$$

$$C_{gfin}=C_{gfin_{top}}+C_{gfin_{corner}}+C_{gfin_{side}}+C_{gfin_{bottom}}$$

Table 1 : capacitances equations summary

References

[1]L. Wei et al, p.1361-1369, TED 2011. [2]W. Wu et al, p.692-698, TED 2007 [3]F. Pregaldiny et al, p.2191-2198, SSE 2002 [4] S. Monfray *et al.*, IEDM 2010 [5] H. Kawasaki *et al.*, IEDM 2009 [6] A. Bansal et al, p.256, TED2005 [7] Plonsey 1961 *Principles and Applications of Electromagnetic Field.* [8]Raphael®, www.synopsys.com[9]www.pdesolutions.com [10] http://itrs.net/ [11]C. Busseret et al SISPAD 2006 [12]D. Garetto et al INC 2010 [13] Fleury, Ph.D. dissertation, 2007.