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A Stacked Inverter-based CMOS Power Amplifier in 65nm CMOS Process

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1. Introduction

In order to develop a single chip radios in CMOS technology, power amplifier is still a bottleneck. With the aggressive scaling down of the gate length in CMOS technology, unlike other blocks which benefit from this advancement, break down voltage reduction makes it more difficult to get high output power from a power amplifier (PA). Oxide breakdown and hot carrier effect are two issues in PAs that originate from voltage stress on the CMOS transistor and get worse as the technology scales. If the power supply is to be reduced, same output power will be achieved by reducing the output impedance by the square value and increasing the current by the same value. The former complicates the matching network and latter will increase loss in parasitic resistors. These facts makes the CMOS power amplifier designing more challenging. In this paper we will describe our method for overcoming the voltage stress issue in CMOS devices [1].

2. Circuit Topology and Principle of Operation

The proposed power amplifier (PA) schematic is shown in Fig. 1. In this circuit in order to reduce the voltage stress on transistors and still achieve a high output power, various techniques have been used.

Inverter-based Topology

As shown in Fig. 2 (a), conventional common source PA needs an inductor and signal swing is twice the supply voltage and hence voltage stress is $2V_{DD}$ across its V_{DS}. Inductors are not desired in CMOS technology since the occupy large area, have low performance and do not scale with technology advancement. Inverter-based PA which is shown in Fig. 2 (b) is an inductorless solution in which V_{DS} will be at most V_{DD} [2].

Self-biased Cascode

Cascode configuration can be used to reduce the voltage stress on each transistor and hence lessening effects of oxide breakdown and hot carrier degradation. Conventional cascode PA is shown in Fig. 3 (a). Under large signal operation, since the gate of M2 is AC grounded, voltage swing at its gate-drain becomes larger than that of M1 and therefore making the common gate transistor the bottleneck of cascode in PA. Shown in Fig. 3 (b), we have used self-biased cascode in order to alleviate the voltage stress across the gate-drain of common-gate transistor. This is done by using a resistor across the gate-drain of M2 which allows the gate to experiences a RF swing in-phase with drain and consequently reduces the voltage stress on M2.

Stacked Structure

The idea of a self-biased cascode has been expanded to a stacked CMOS structure. In this structure several transistors are connected in series in order to achieve high output voltage while keeping the voltage on each CMOS as low as satisfying the breakdown voltage condition.

3. Fabricated Chip and Measurement Results

To prove the concept, a three stage stacked inverter-based CMOS PA was fabricated in 65nm CMOS technology. VDD in Fig. 1 was set to 1.2 V, therefore first, second and third stages use 2.4 V (VDD1), 2.4 V (VDD2) and 6 V (VDD3) of power supply respectively. Fig. 4 shows the microphotograph of the fabricated PA which occupies 0.11 mm^2 of area. Shown in Fig. 5 is measured S parameters of the PA. In order to measure the linearity of PA, two-tone test was carried out at 1 GHz and 2 GHz which its results is shown in Fig. 6. Table 1 shows some selected parameters of PA. Since it was a two-tone test P_{1dB} and P_{sat} (output power at saturation) is about 3dB higher than that of two-tone test results. Note that 16dBm of saturated output power means that output pick to pick voltage swing is 4 V_{pp} and yet there is no voltage stress on the transistors which clearly points to the usefulness of stacked structure for reliable power amplifier implementation.

4. Conclusions

In this work, we proposed a stacked inverter-based CMOS PA which is alleviating oxide breakdown and hot carrier degradation effects by reducing the voltage stress on each transistor while generating high output power. Employing inverter-based structure, this PA does not need any inductor as RF choke.

Acknowledgements

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References

[1] T. Sowlati and D. M. W. Leenaerts, "A 2.4-GHz 0.18-µm CMOS Self-Biased Cascode Power Amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1318–1324, Aug. 2003.

[2] K. Y. Son, C. Park and S. Hong, "A 1.8-GHz CMOS Power Amplifier Using Stacked nMOS and pMOS Structures for High-Voltage Operation," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 11, pp. 2652–2660, Nov. 2009.

Table 1 Measured parameters of PA

	P_{1dB} (dBm)	P_{sat} (dBm)	Small signal gain (dB)
1 GHz	13.3	16	36
2 GHz	12.9	14.3	30

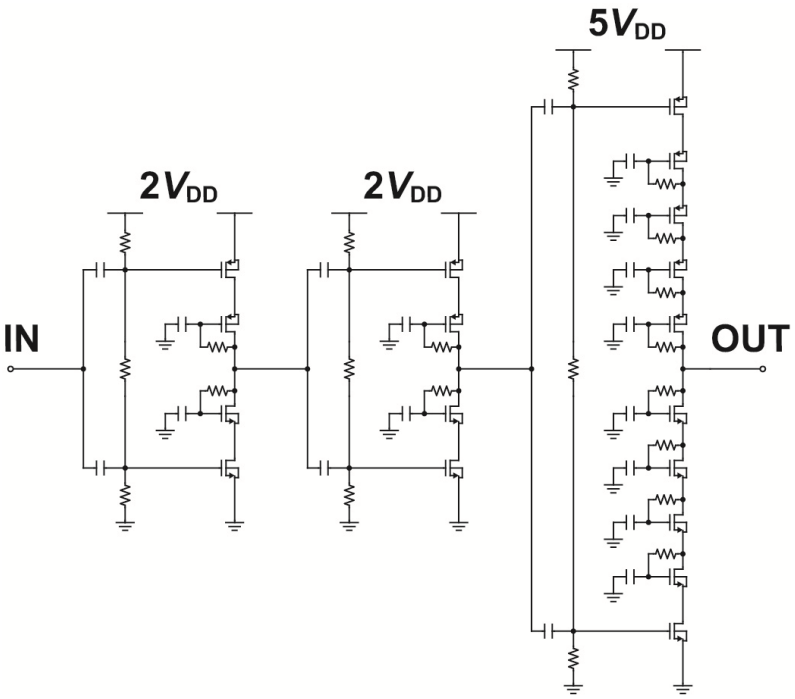
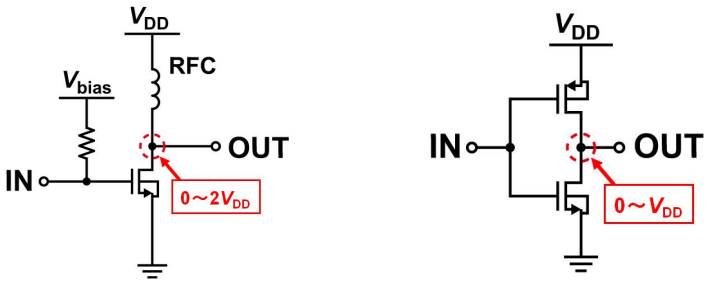
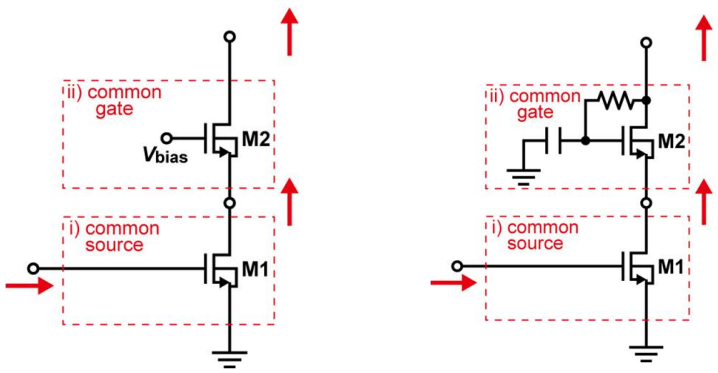


Fig. 1 Schematic of the proposed stacked PA



(a) (b)

Fig. 2 (a) Conventional PA (b) Inverter-based PA



(a) (b)

Fig. 3 (a) Conventional cascode (b) Self-biased cascode

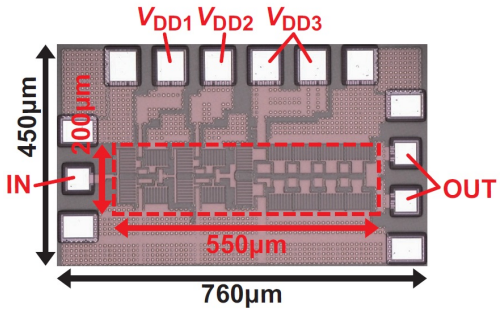


Fig. 4 Microphotograph of the fabricated CMOS PA

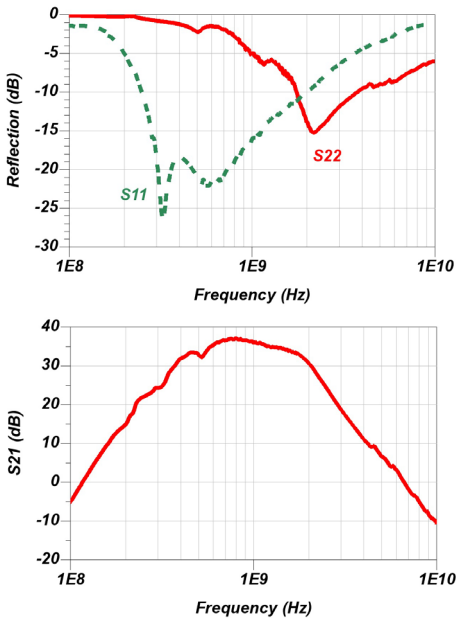


Fig. 5 Measured S parameters

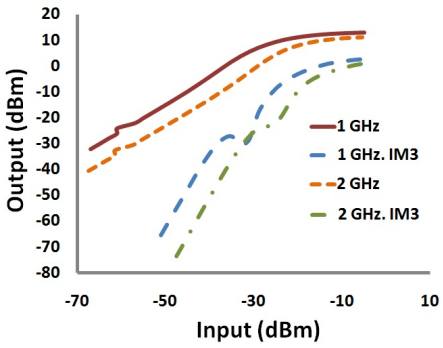


Fig. 6 Measured two-tone test of PA at 1 GHz and 2 GHz