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Design of Power-Efficient 130GHz Common-Source Amplifiers

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1. Introduction

A D band (110-170GHz) is a promising band for next-generation transceivers [1]. Designing a CMOS millimeter -wave amplifier is a key to realizing low-power and cost-effective transceivers in this band. Thus, many studies have been reported [2, 3]. Indeed, CMOS technology contributes the reduction of power consumption; nonetheless, the power consumption is becoming higher as reported previously and shown in Fig. 1 because the maximum available gain (MAG) of MOSFET is degraded as a function of -20dB per decade of frequency, and square power is required to compensate for it. That is an issue. Thus, even in a CMOS process, a power-efficient design is required, particularly at higher frequencies. In this paper, we provide a new tool for optimizing the power consumption under the desired total gain with a sacrifice of total area. The main idea is identify an optimum drain current controlled by supply and gate bias voltages at each stage of a common-source amplifier. In section 2, an index of power efficiency and its equations are introduced. In section 3, actual optimization is shown utilizing the measured data of a fabricated common-source MOSFET. In section 4, an applied design is demonstrated in comparison with the conventional one.

2. Power-Efficient Design

Fig. 2 shows an *n*-stage amplifier. Its total gain *nG* per total *nP* is the same as the single *G*-*P* ratio. Thus, maximizing the *G*-*P* ratio is important for power-efficient amplifier design. Fig. 3 shows a MAG of MOSFET related with power consumption. MOSFET was biased at a point that achieves the highest MAG to obtain the highest f_{max} [2] (MAG-max bias). However, much power is consumed at the MAG-max point. As shown in Fig. 3, there should be a biasing point at which not much power is consumed but there is still gain (power-conscious bias). This point maximizes the MAG per power consumption. The gain of the power-conscious point is lower than that of the MAG-max point. In a more practical circuit than that shown in Fig. 2, the loss between the amplifiers should be considered. Fig. 4 shows a two-stage common-source amplifier. It has a couple of MOSFETs as active elements and they and I/O ports are connected with matching networks. Each active element has a gain *G*, which can be assumed as MAG if the matching network is designed properly, and consumes power *P*. The matching network facing I/O ports has a loss whose value is half that between MOSFETs'. In the case of *G*, *P* and *L* have the same values. The total power consumption P_{total} and total gain G_{total} of an *n*-stage common-source amplifier can be described as

$$P_{total} = nP, \quad (1)$$

$$G_{total} = n(G - L). \quad (2)$$

Using the above equations, the power efficiency is defined as

$$G_{total}/P_{total} = (G - L)/P. \quad (3)$$

This equation implies that the total gain G_{total} per supplied power P_{total} is not related with the number of stages *n*. Thus, power-efficient design requires optimizing just one stage by controlling the voltages of power supply V_{ds} and bias V_{gs} shown in Fig. 4 without considering the number of stages *n*.

3. Measurement and Optimization

To ensure the above condition, MOSFET was fabricated using 40nm CMOS technology (Fig. 5) and measured. Its W/L = 32μm/44nm and its gate, drain and source are connected to port1, port2 and grounds, respectively. Its gate bias and supply voltages are fed via bias tees on port1 and port2. After measuring S-parameters at 130GHz using VNA, MAGs were calculated and the supply current was measured as well. Fig. 6 shows the MAG and power consumption, calculated from supply currents and voltages, with respect to the gate bias voltage while the supply voltage is 1.1V (upper limit of this process). The largest MAG is 6.39dB at 0.75V gate bias V_{gs} with 11.0mW power consumption *P*. The MAG-max design picks this point up. However, from viewpoint of Eq. 3, the efficient gate bias is different. Fig. 7(b) shows the $(G - L)/P$ with respect to the gate bias V_{gs} when *L* = 1dB. The solid line and dashed lines indicate the case of V_{ds} = 1.1V, 0.8V and 0.6V, respectively. There is an optimum point (V_{gs} = 0.52V) for V_{ds} = 1.1V, and the points exist for each power supply voltage V_{ds}. The optimum point does not necessarily exist on the allowed highest voltage supply (V_{ds} = 1.1V). Fig. 7shows the power-conscious bias point for each loss *L* of matching network. Fig. 7 reveals that the bias point depends on the loss *L*. If the loss *L* becomes larger, it becomes harder to compensate it using gain *G* of each MOSFET with a lower power supply voltage V_{ds}.

4. Comparison with Conventional Design

After finishing the bias and supply voltage optimization of a single stage, it is ready to try to meet the desired total gain G_{total} by increasing the number of stages *n*. Fig. 8

shows the total power consumption P_{total} related with the total gain G_{total} in the case of the matching network having 1dB loss (the number of stages are indicated on the line). In Fig. 8, for instance, if the total gain requirement is over 10dB, the conventional method (MAG-max bias) achieves it in two stages with 22.0mW power consumption. On the other hand, the proposed method (power-conscious bias) achieves it in four stages with 8.4mW. Thus, in this case, the proposed method reduced by 62% the power consumption relative to that of the conventional method.

5. Conclusions

In this paper, we introduced a novel method of optimizing CMOS millimeter-wave amplifiers. By applying this method to a certain case, the power consumption of an amplifier is markedly reduced. Since this method tends to increase the number of stages, the area of amplifiers may also be increased. Moreover, to utilize this method effectively, designing low-loss matching networks is important.

Acknowledgements

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References

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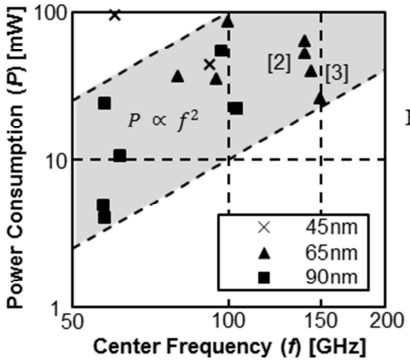

Fig. 1. Power consumption of millimeter-wave CMOS amplifiers as a function of operation frequency.

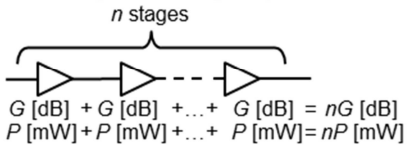

Fig. 2. Relationship between power consumption and gain of a multi stage cascade amplifier.

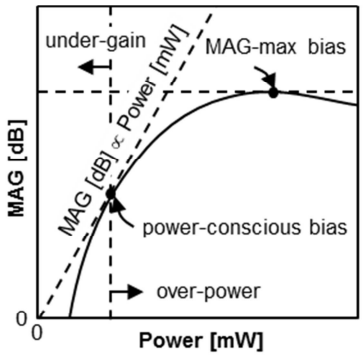

Fig. 3. Bias points of a common-source circuit. A bias is conventionally adjusted at the point where MAG becomes highest (MAG-max bias). On the other hand, power consumption is reduced when a bias is adjusted at the point where MAG per power becomes highest (power-conscious bias).

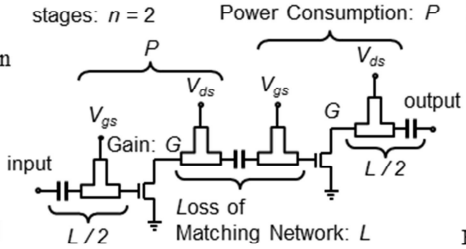

Fig. 4. Schematic of a two-stage common-source amplifier where losses in matching networks are considered.

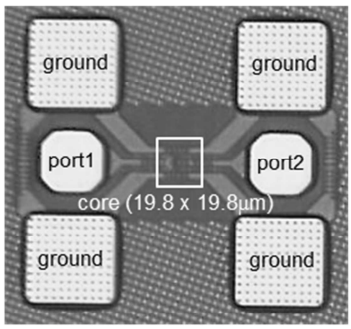

Fig. 5. Micrograph of a MOSFET used for measurement.

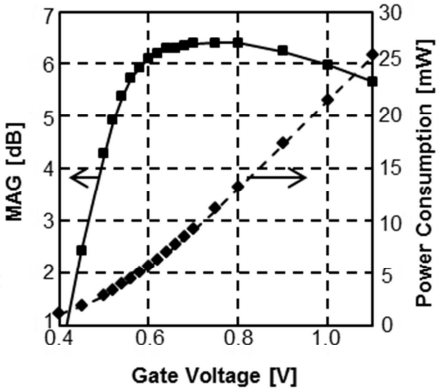

Fig. 6. MAG and power consumption of a MOSFET as functions of gate voltage (V_{gs}) when drain voltage (V_{ds}) is 1.1V and frequency is 130GHz.

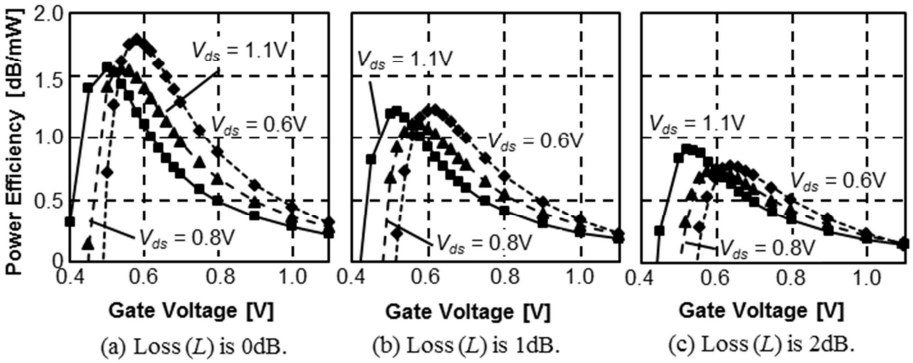

Fig. 7. Power efficiency (=(MAG - L)/power) as a function of gate voltage taking account of a loss of matching networks, where frequency is 130GHz and V_{ds} are 0.6V, 0.8V, and 1.1V.

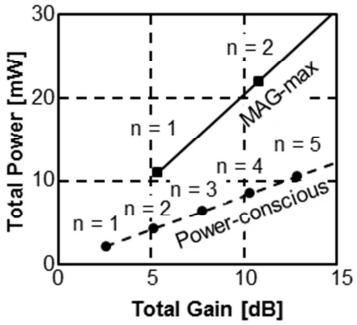

Fig. 8. Total power consumption of 130GHz multi stage CMOS amplifiers as functions of the total Gain.