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Current Drive Enhancement of Strained Ge nMISFET with SiGe Stressors by Uniaxial Tensile Stress

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1. Introduction

Ge channel MISFETs have been proposed as a promising candidate of future device structures over the scaling limit of Si technology, because of the higher carrier mobility than Si (two times for electrons and four times for holes). Channel strain engineering is currently very successful in Si MISFETs in terms of the enhancement of carrier mobility and transistor performance. It has been theoretically reported [1] that electron mobility enhancement of Ge channel by introducing uniaxial strain. Moreover, the effect of the tensile strain on Ge nMISFET performance was also reported by using bending apparatus [2] [3]. These result concluded that the uniaxial tensile strain enhanced the electron mobility of Ge nMISFETs, similar to Si nMISFETs. Most desirable approach to introduce uniaxial tensile strain in the Ge channel is through the integration of SiGe source and drain (S/D) with a smaller lattice constant than Ge. SiGe S/D can be easily integrated in Ge nMISFETs [4], similar to the integration of Si:C S/D in Si nMISFETs [5]. In addition, higher strain is induced in the channel with a smaller gate length (L_g) with SiGe stressor.

In this paper, we investigate the current drive enhancement of strained Ge nMISFET introducing uniaxial tensile strain by employing SiGe S/D stressor for the first time.

2. Experimental

The device fabrication flow is shown in **Fig. 1**. The substrates used in this study were pGe (001) (~0.1Ωcm). After device isolation, 6nm thick CVD-SiO_2 was deposited as a gate dielectric after deposition of 7ML Si passivation layer [6] without implantation of channel impurity ions. TaN and a-Si were sputtered as a gate electrode. The gate patterning was done by E-beam lithography process with a SiO_2 hard mask. After SiO_2 sidewall formation, recess structures were etched by wet solution. Next, SiGe Selective Epitaxial Growth (SEG) was applied on the recess regions. The Ge composition, x, of SiGe stressor was 0.7, 0.8 and 1.0 (Ge) [7]. During SEG, hardmask and sidewalls covered metal gate. P^+ implantation was carried out to the S/D regions. After activation anneal (500°C), BEOL process was performed at the maximum temperature of 420°C. On the control wafer, the Ge recess etching and SEG were not performed. The strain applied in Ge channel layers was measured with micro-Raman spectroscopy by using the SiO_2 dummy gate samples [7].

3. Results and Discussion

Fig. 2 shows cross-sectional transmission electron microscopy (TEM) images of the nMISFET after SiGe (x = 0.7) SEG. 50nm-thick embedded SiGe stressor was clearly observed. From this image, it is also confirmed that sidewall length (L_{sw}) is about 25nm.

Fig. 3 shows (L_g+2L_{sw}) dependence of average uniaxial tensile strain in Ge channel regions with the SiGe stressors. These values were estimated from the Raman peak shifts for the Ge-Ge vibration mode, according to the manner published in [8] [9]. It is confirmed that the values of uniaxial tensile strain increase with decreasing (L_g+2L_{sw}), and *x* of SiGe stressors. The tendency is consistent with that for Si-MOSFETs with Si:C stressors [10].

I-V curves of n^+Ge/pGe and n^+SiGe/pSiGe diodes are shown in **Fig. 4**. These diodes exhibit rectifying characteristics over the range of *x* of the SiGe stressor. The reverse current is, however, becomes higher for lower *x*. This result may be attributed to defects near the SiGe/Ge interface.

Fig. 5 and **Fig. 6** show I_s-V_g characteristics for nMISFET with SiGe (*x* = 0.7) stressor. In L_g = 1μm device, I_{ON}/I_{OFF} ratio of 3 orders of magnitude was obtained. Although I_{ON}/I_{OFF} ratio and Subthreshold Slope (SS) were significantly degraded for shorter L_g devices due to the thick EOT and the low channel-impurity concentration, FET operation has been observed down to 50nm L_g as shown in **Fig. 6**.

In order to estimate the effect of local tensile strain on the current drive, the maximum transconductance (Gm_{max}) was extracted as a function of L_g. **Fig. 7** compares the L_g dependence of the normalized Gm_{max} in the linear regime, which is defined as $Gm_{max}(L_g)$ / $Gm_{max}(L_g = 1\mu m)$. It was found that the enhancement factor of the normalized Gm_{max} against the control devices was increased for shorter L_g devices and was amounted to be 1.3 and 1.6 at L_g = 50 nm for *x* = 0.8 and *x* = 0.7, respectively. Electron mobility enhancement factors of 1.6 and 2 against an unstrained (001) Ge nMISFET are estimated [1] from the measured uniaxial tensile strain values of 0.4% and 0.6% for *x* = 0.8 and *x* = 0.7 devices at L_g = 50nm (i.e. L_g+2L_{sw} = 100nm), respectively, as shown in **Fig. 3**. The obtained linear Gm_{max} enhancements are reasonable considering the mobility enhancement factors. The deviation may be due to high parasitic S/D resistance of the present devices. In the saturation regime, the enhancement factor of the normalized Gm_{max} was decreased (**Fig. 8**) but the values were almost consistent with a relation of $I_{dsat} \propto \mu^{0.5}$ [11] [12] as shown **Fig. 9**. The result suggest that the current drive enhancement for short channel devices is originated from the tensile strain in the Ge channel adjacent to the SiGe S/D stressors.

4. Conclusions

Fabrication of the strained Ge nMISFETs having SiGe S/D stressors with L_g down to 50nm and the strain-induced current drivability enhancement were successfully demonstrated. The Gm_{max} enhancement factor of strained SiGe S/D nMISFETs was found to be consistent with the measured strain dependences on Lg and *x* in SiGe S/D. These results suggest that uniaxial tensile strain generated by SiGe S/D stressors is effective for the performance booster of scaled Ge nMISFET.

Acknowledgements

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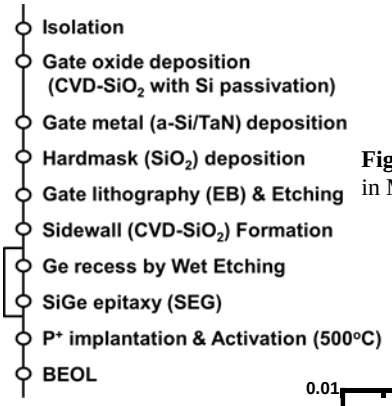

Fig. 1 Process flow employed in MISFET fabrication.

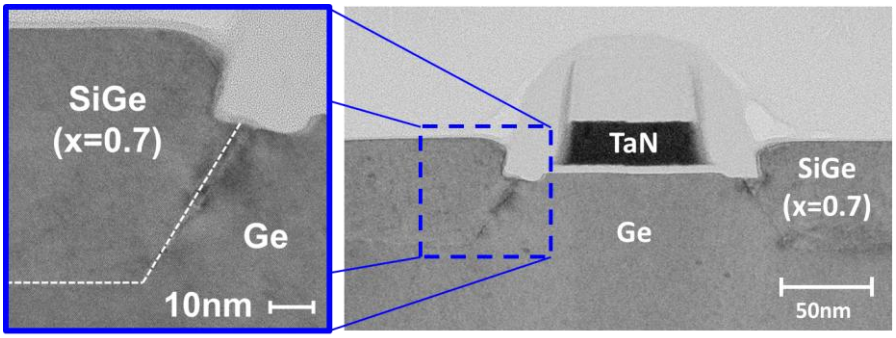

Fig. 2 Cross-sectional TEM image of nMISFET with SiGe(x = 0.7) stressor.

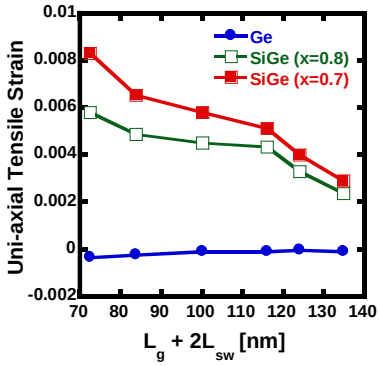

Fig. 3 (L_g+2L_{sw}) dependence of uniaxial tensile strain of Ge channel with SiGe stressor.

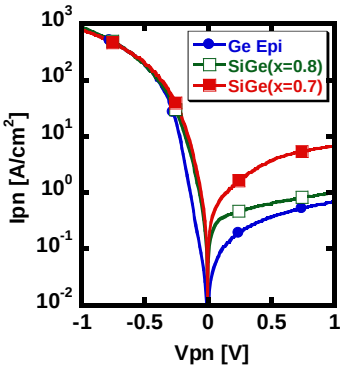

Fig. 4 I-V curves for the n^+Ge/pGe and n^+SiGe/pSiGe diodes.

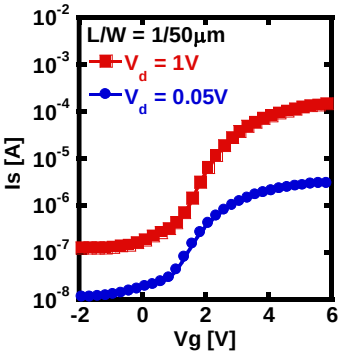

Fig. 5 I_s-V_g characteristics of L_g=1 μm nMISFET with SiGe(x = 0.7) stressor at V_d = 0.05 V and 1 V.

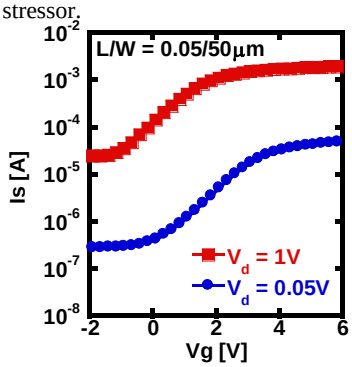

Fig. 6 I_s-V_g characteristics of L_g=50 nm nMISFET with SiGe(x = 0.7) stressor at V_d = 0.05 V and 1 V.

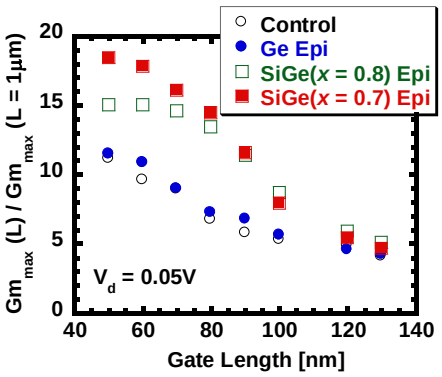

Fig. 7 The normalized Gm_{max} as a function of L_g at V_d = 0.05V. The normalized Gm_{max} of SiGe(x = 0.8) and SiGe(x = 0.7) S/D device shows ~31% and ~61% gain over the control device at L_g = 50nm, respectively.

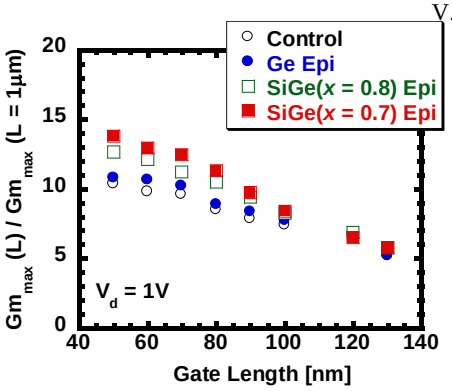

Fig. 8 The normalized Gm_{max} as a function of L_g at V_d = 1V. The normalized Gm_{max} of SiGe(x = 0.8) and SiGe(x = 0.7) S/D device shows ~18% and ~28% gain over the control device at L_g = 50nm, respectively.

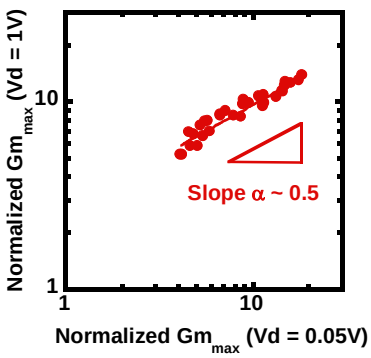

Fig. 9 The Linear normalized Gm_{max} dependence of the saturation normalized Gm_{max}. The power of the linear normalized Gm_{max} dependence is about 0.5.