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Lateral Source Relaxed/Strained Layer Heterostructures for Ballistic CMOS : Physical Relaxation Mechanism for Strained Layers by O^+ Ion Implantation

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I. Introduction

We have experimentally demonstrated high velocity electron injection into the channel from the source in n-channel source heterojunction MOS transistors (SHOTs) for a future ballistic CMOS, utilizing the excess kinetic energy corresponding to the conduction band offset, ΔE_C at the source-relaxed SiGe/channel-s-Si heterojunction [1]. To realize p-SHOTs as well as the abrupt heterojunction to increase the injected carrier velocity, we have demonstrated a new abrupt lateral source-heterojunction with relaxed/strained semiconductor layers on a single semiconductor substrate by O^+ ion induced relaxation technique of strained layers due to the O^+ recoil energy, E_R at the strained layer/buried oxide layer (BOX) interface [2], [3].

In this work, we have experimentally studied the relaxation mechanism for the strained layer on the BOX, using local O^+ ion implantation into the strained Si (s-Si) on the BOX (SSOI) substrates and the post annealing process. We have experimentally shown the critical annealing temperature as well as the critical E_R for relaxing the strained layers, and then have clarified a physical mechanism for relaxing the strained layers. Moreover, we have discussed the device design for SHOTs, by showing the crystal quality of the lateral relaxed/strained layer heterojunction.

II. Concept for Source Heterojunction CMOS Structures

Fig. 1 shows n-SHOT structures [2]. Local relaxed-source layers can be simply fabricated by local slip of the strained layers on the BOX interface due to optimized E_R distribution by SRIM [4].

We have experimentally demonstrated that both SSOI and SGOI substrates are suddenly relaxed at the critical value of E_R, E_{RC} [2]. Moreover, we have successfully formed an abrupt lateral strain distribution of the relaxed/s-Si heterostructures [3]. As a result, the conduction band offset $\Delta E_C(\equiv E_C - \Delta_2)$ between relaxed/s-Si layers can be achieved. Using the ΔE_C, an ideal carrier velocity enhancement Δv can be expressed by $\Delta v=(2\Delta E_C/m_T^*)^{1/2}$, where m_T^* is the transverse effective mass of inversion carriers of the channel.

III. Relaxation Mechanism for Strained Layers

We have carried out the post furnace annealing process for 30min. at various temperatures T_A only after a conventional room temperature O^+ ion implantation into the 0.7% strained SOIs with the s-Si thickness T_{SS} of 60-nm and 13-nm. In order to evaluate the strain of thin s-Si layers, we have carried out UV(325-nm)/visual(532-nm) Raman spectroscopy with the laser beam diameter of about 1 μm.

Fig. 2 shows the O^+ ion dose, D_O dependence of the relaxation rate, R of SSOIs fabricated by conventional (25°C) or hot (950°C) O^+ ion implantation processes for 30min. Therefore, the total thermal budget of both the conventional and the hot O^+ ion implantation processes is the same. In both O^+ ion implantation processes, the SSOIs are suddenly relaxed at the critical O^+ ion dose, D_{OC} of about 2×10^{15} cm^{-2} ($E_{RC}\approx3\times10^{16}$eV/cm^2) [3]. The R of s-Si formed by the conventional O^+ ion implantation rapidly increases with increasing D_O higher than D_{OC}. However, the R of s-Si fabricated by the hot O^+ ion implantation is much lower than the R of s-Si formed by the conventional O^+ ion implantation, which is probably due to rapid recovery of the broken bond between the s-Si/BOX layers during the high-temperature process in the hot O^+ ion implantation. Therefore, the density of the broken bond between the s-Si/BOX by the O^+ ions, D_{BB} is required to be higher than the critical value of D_{BB}, D_{BBC} to relax the s-Si layers only by the conventional O^+ ion implantation.

Moreover, Fig. 3 shows the T_A dependence of the R of s-Si. When the T_A is higher than the critical annealing temperature T_{AC} of about 650°C, the s-Si layers are suddenly relaxed. Therefore, the critical thermal-stress during the post annealing process is required to slip the s-Si layers on the BOX. However, the R evaluated by the visual Raman spectroscopy with the penetration length, $L_P\approx$1-μm is higher than the R by UV Raman spectroscopy with $L_P\approx$5-nm, which indicates that the s-Si layers are much relaxed at the s-Si/BOX interface, compared with the surface s-Si layers, as shown as the inset of Fig.3. In addition, Fig.4 also shows the T_A dependence of the R of s-Si as a parameter of the D_O. It is noted that the T_{AC} actually exits in both D_O conditions. However, the T_{AC} at higher D_O condition is lower than that at lower D_O. Namely, the T_{AC} decreases with increasing D_O, which means that the D_{BB} generation increases with increasing D_O, resulting in the R increase of the s-Si layers.

Fig.5 shows the 2D mapping distribution of the R of the O^+ ion (3×10^{15}cm^{-2}) implanted s-Si layers at T_A =950°C and clearly proves the very uniform R distribution, where the standard deviation of the R is only 1% in a 200 square μm^2 area.

According to the above discussion of Figs. 2-4, we have clarified a two-step relaxation mechanism for strained layers, as shown in Fig.6. Fig. 6(a) shows the first step for generating D_{BB} at the strained semiconductor/BOX interface due to the E_R of implanted O^+ ions, and then, Fig. 6(b) shows the second step of the slip of the strained semiconductor on the BOX layer caused by the thermal stress during the post annealing process. Thus, it is necessary to carry out both the post-annealing and the conventional O^+ ion implantation processes, to realize a higher R of the strained layers.

IV. Crystal Quality of O^+ Ion Implanted Strained Layers

Fig.7 shows the TEM image of the cross section of the O^+ ion implanted s-Si layers with and without optimizing the E_R peak depth, R_{ER}. The clear lattice image is observed in the optimized E_R condition in Fig. 7(a), but we have observed a lot of dislocations in Fig. 7(b). Therefore, the crystal quality of the ion implanted layers with the optimized E_R condition is not degraded in spite of high dose O^+ ion implantation process, because the depth E_R profile of the O^+ ion can be controlled to be rapidly reduced in the s-Si layer and have the peak value at the s-Si/BOX interface [2].

Moreover, Fig 8 shows the T_A dependence of the crystallization rate R_C determined by the half width of Raman peak of s-Si, where the half width is an indicator for the Si crystalline quality. Here, $R_C=W_{HI}/W_H$, where W_H and W_{HI} are the half width of Raman peak of the ion implanted s-Si and the initial SSOIs, respectively. The R_C can be recovered at higher T_A condition and becomes higher than 0.9 when T_A>600°C at lower D_O condition. However, the R_C is degraded at higher D_O condition. Moreover, Figs. 9(a) and (b) show the TEM image of the plane view of the initial s-Si surface and the s-Si after D_O of 1.5×10^{15} cm^{-2} and the post annealing processes, respectively. Compared with Fig. 9(a), Fig. 9(b) shows a good quality of the O^+ ion implanted s-Si layers with the R of 50%, although we observed a very small area with amorphous Si (a-Si) layers shown as the bright areas.

V. Buffer Layer between Lateral Relaxed/Strained Layers

We carried out TEM observation of the cross section of the O^+ ion implanted s-Si layers near the 50-nm length gate mask edge, as shown in Fig. 10(a). We have observed the threading dislocation with the angle θ=60° outside the mask edge between the relaxed Si and the s-Si layers. Fig. 10(b) shows the uniform lateral strain value distributions of both the s-Si area under the gate mask and the relaxed region outside the gate mask, which are evaluated by FFTM (Fast Fourier Transform Mapping) analysis. The strain distribution show the direct demonstration that the s-Si under the 50-nm gate can still maintain the initial strain value of SSOIs. In addition, as shown in Fig. 10(c), the dislocation area in Fig.10(a) acts as the buffer layer to form the abrupt lateral-relaxed/strained layer heterojunction reported in our previous paper [3]. The buffer layer length L_B can be expressed as $L_B\approx2T_{SS}\cdot\tan\theta\approx1.15T_{SS}$. As a result, L_B is very short and can be scaled by scaling T_{SS}. Moreover, the buffer layer with the 60°-dislocation will be located within the diffused n^+ layer, as shown in Fig. 10(c). Therefore, the dislocation induced leakage current can be neglected and this source heterojunction edge position in Fig.10(a) is optimized to realize higher Δv in SHOTs [1].

VI. Conclusion

We have experimentally clarified the relaxation mechanism for the strained layer on the BOX, using the conventional/hot O^+ ion implantation and the various post-annealing-temperature processes. The strained layers can be relaxed by a two-step relaxation mechanism with 1st step of breaking the bond between the strained layer/BOX interface by the O^+ ions and the 2nd step of the slip of the strained semiconductor on the BOX layer caused by the thermal stress during the post annealing process.

Moreover, according to high crystal quality of the lateral abrupt-relaxed/strained layer heterostuctures, the local O^+ ion implantation induced relaxation technique is very promising for nano-scaled CMOS SHOTs.

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References: [1] T.Mizuno, *VLSI Symp.*, p.22, 2008. [2] T.Mizuno, SSDM, p.769, 2009. [3] T.Mizuno, SSDM, p.45, 2010. [4] J.F.Ziegler, http://www.srim.org/.

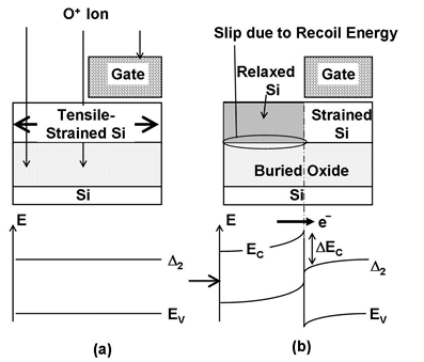

Fig.1 n-channel SHOT structures with source relaxed Si/tensile-s-Si heterojunction, fabricated by source O^+ ion implantation. Δ_2 is the energy level of the 2-fold valley of the s-Si, and E_C and E_V are the conduction and the valence band levels, respectively.

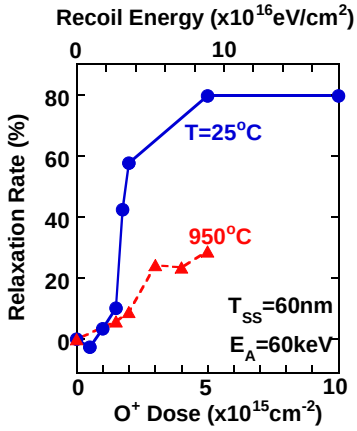

Fig.2 D_O and E_R at s-Si/BOX interface dependence of relaxation rate of strained layers fabricated by room temperature (circles) or hot (950°C) (triangles) O^+ ion implantation process, where SSOI thickness, T_{SS}=60nm and activation energy, E_A=60keV. Post-annealing at 950°C was carried out only after the room temperature O^+ ion implantation.

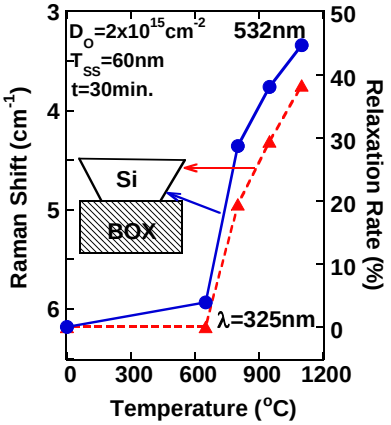

Fig.3 Annealing temperature dependence of the relaxation rate of strained layers by evaluated by a 325-nm (triangles) and a 523-nm (circles) wavelength Raman spectroscopies, where T_{SS}=60nm, E_A=60keV, D_O=2×10^{15} cm^{-2}, and annealing time, t=30min.

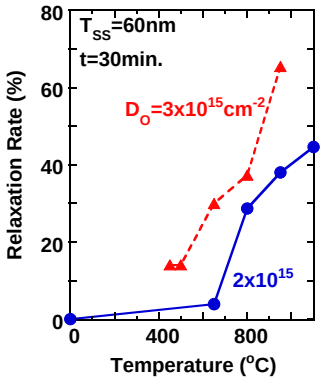

Fig.4 Annealing temperature dependence of relaxation rate of strained layers by evaluated by a visual Raman spectroscopy, where T_{SS}=60nm, E_A=60keV, and t=30min. Circles and triangles show the data at D_O=2×10^{15} cm^{-2} and 3×10^{15} cm^{-2}, respectively.

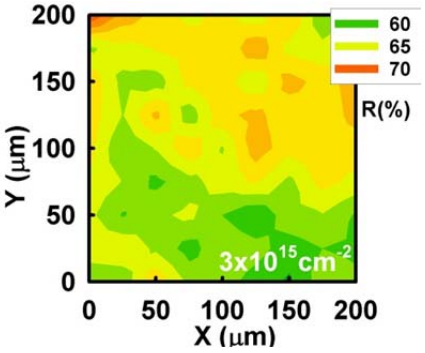

Fig.5 2D mapping (200μm square area) of R, where T_{SS}=60nm, D_O=3×10^{15}cm^{-2}, E_A=60keV, and T_A=950°C. The average R and the standard deviation are 65.5% and 1.0%, respectively.

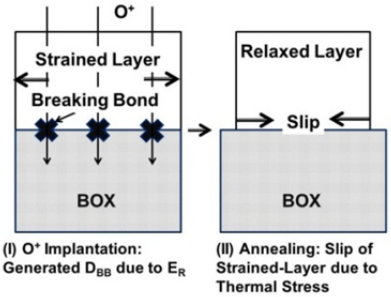

Fig.6 Two-step relaxation mechanism for strained layers by (I) 1st step of D_{BB} formation by O^+ ion implantation and (II) the 2nd step of slip by post annealing processes.

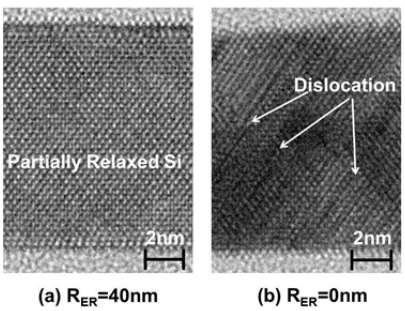

Fig.7 TEM image of cross section of an O^+ ion implanted s-Si layers (a) with and (b) without optimizing E_R profile of the R_{ER}, where T_{SS}=13nm, D_O=1.5×10^{15} cm^{-2}, T=950°C, and t=30min. (a) R_{ER}=40 nm and (b) R_{ER}=0 nm. The R of Fig. (a) is about 50%.

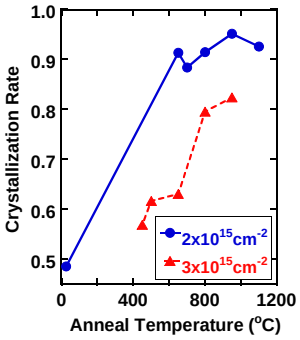

Fig.8 Annealing temperature dependence of crystallization rate of ion implanted s-Si regions. The circles and the triangles show the data of D_O=2×10^{15} cm^{-2} and 3×10^{15} cm^{-2}, respectively.

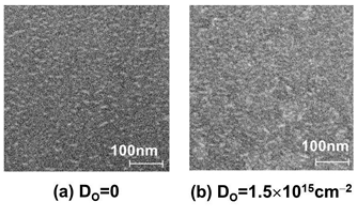

Fig.9 Plane TEM image of (a) an initial s-Si layer and (b) an O^+ ion implanted s-Si layer with relaxation rate of 50%, where T_{SS}=13nm, E_A=25keV, D_O=1.5×10^{15} cm^{-2}, T=950°C, and t=30min. Small area, shown as the bright regions, shows amorphous Si layers.

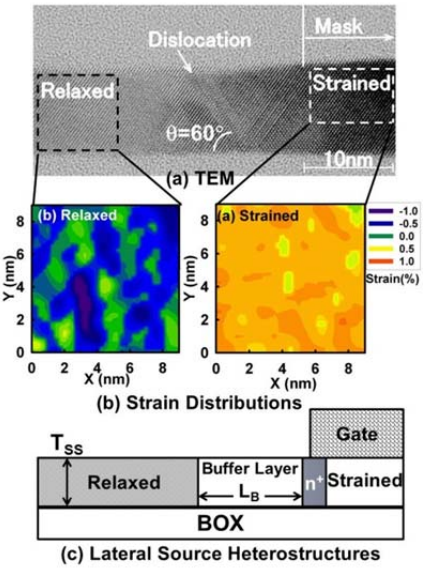

Fig.10 (a) TEM image of cross section of an O^+ ion implanted s-Si layer with relaxation rate of 50% near the 50-nm length gate mask edge, where T_{SS}=13nm, E_A=25keV, D_O=1.5×10^{15} cm^{-2}, T=950°C, and t=30min. The arrow shows the threading dislocation with θ=60°. (b) Lateral strain value distributions of the strained region under the SiO_2 mask and the relaxed region outside the SiO_2 mask which are evaluated by FFTM. The lateral strain values of the strained and the relaxed regions are about 0.65±0.1% (tension) and -0.26±0.27% (compression), respectively. Therefore, the 50-nm length strained regions can still maintain the initial strain value of the SSOIs. The ion implanted regions are relaxed, and the partial areas are compressively strained. (c) Schematic cross section of source heterostructures with the buffer layer between relaxed and strained layers. L_B shows the length of a buffer layer, resulting in $L_B \approx 2T_{SS}\tan\theta \approx 1.15T_{SS}$. L_B is only 15nm in this work. The buffer layer with the dislocation will be located within the diffused n^+ layer.