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Recovery Characteristic of Anomalous Stress Induced Leakage Current of 5.6nm Oxide Films

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1. Introduction

Downscaling of metal oxide semiconductor field effect transistors (MOSFETs) is very important for the large integration of memory device. However in the flash memory, stress induced leakage current (SILC) induced by Write / Erase cycling imposes the limitation of downscaling of the tunnel oxide thickness [1]. Furthermore thinning of tunnel oxide leads to a higher appearance probability of anomalous SILC which is some order of magnitude larger than average SILC [2,3]. These anomalous SILC causes severe bit error in flash memory and also limit the downscaling of oxide thickness. The recovery of anomalous SILC has been reported which depends on the applied electric field or/and temperature [3]. The recovery of anomalous SILC is a serious issue because it makes the evaluation of the bit error very difficult, however the detail mechanisms of these phenomena have not been understood. In this paper we discuss the recovery characteristic of anomalous SILC of thin oxide films in time domain, which is important to understand the characteristics of anomalous SILC.

2. Experimental

In this experiment, gate oxides were formed by 850ºC wet oxidation, and to generate anomalous SILC effectively we used a relatively thin oxide (5.6nm) for the evaluation. The gate area is $1\mu m^2$. This device size was determined to prevent anomalous SILC from being hidden by the average gate current. A constant electric field stress (10MV/cm) is applied up to 10^4 sec to MOSFETs to generate anomalous SILC. We have already succeeded in measuring gate leakage current of a large number of MOSFETs accurately in a short measurement time by using the array test pattern reported in [3]. The test pattern can measure gate leakage current with 10^{-16}A order for 87,344 MOSFETs continuously with the sampling time of several tens of seconds. After the electric filed stress, gate leakage current was measured in the time domain for five days at 25ºC in order to analyze the recovery characteristic of anomalous SILC. In this experiment, the sampling period is 83sec.

3. Results and Discussion

Fig.1 shows the distributions of gate leakage current of 87,344 MOSFETs at various stress time. The tail distribution in the Gumbel plot increases with an increase of stress time. In these tail parts, there are anomalous SILCs of which current are over one order of magnitude larger than the average SILC.

Fig.2 shows the distributions of gate leakage current of 87,344 MOSFETs measured after the stress for five days. The gate current of tail and main distributions decreased with an increase of time after the stress.

Fig.3 shows Ig-Eox characteristics of anomalous SILCs and average SILCs. The currents were decreased as time after stress increased for both cases. Fig.3(a) shows the typical cell in which the anomalous SILC did not recover in 12 hours. The amount of decrease in anomalous SILC after the stress is almost the same as that of the average SILC. This means that the anomalous SILC did not decrease with time in this cell. It is considered that the leakage spot of the anomalous SILC is much smaller than the cell area of $1\mu m^2$. Fig.3(b) also shows the another typical anomalous SILC which suddenly changes down to the average SILC after 2 hours. This discrete change suggests that a few traps in the oxide cause the anomalous SILC, and we consider that recovery characteristic is caused by either of phenomena, (i) screening of critical leakage path by one or a few trapped electron(s) or (ii) one or a few hole trap(s) which cause anomalous SILC is emitted from the oxide.

Figs.4-6 show typical examples of transient characteristics of anomalous SILCs measured for about 3 days after the stress. In the Fig.4 anomalous SILCs suddenly changes to the average level. These phenomena also suggest that the anomalous SILC is occurred by a few traps in the oxide. Fig.4(a) and (b) show anomalous SILC without and with random telegraph signal (RTS) [4]. Fig.5 shows anomalous SILCs (a) without RTS and (b) with RTS, which did not recover in 5 days after the stress. Fig.6 shows generation characteristics of anomalous SILCs (a) without RTS and (b) with RTS. Note that the time constant of RTS of gate current shown in Fig.6(a) may be as long as the measurement time. This result suggests that long measurement time is essential for further understandings of anomalous SILC and its RTS characteristics.

Fig.7 shows the number of anomalous SILCs as a function of measured time after the stress. The numbers of anomalous SILCs with and without RTS are also plotted respectively. Note in this experiment the sampling time is 8,300 sec and the gate current of anomalous SILC is defined as gate current which is larger than ($\langle I_G \rangle + 6\sigma I_G$), where $\langle I_G \rangle$ and σI_G are average and standard deviation of gate current of 87,344 MOSFETs respectively. After the measurement time of five days, the remained anomalous SILCs with RTS are less than those without RTS indicating the cell with RTS have higher probability of recovery. It is considered that the more interaction between traps in oxide and Si/SiO_2 interface increases, the more probability of anomalous SILC recover to the average level.

4. Conclusion

The discrete recovery characteristics of anomalous SILC are observed in the time domain. And the anomalous SILC suddenly changes to the average SILC with time after stress. The obtained results suggest that a few traps cause the anomalous SILC. The correlation between the recovery characteristic and the existence of RTS in anomalous SILC is observed. The obtained characteristics are very important for the understanding of anomalous SILC, and these help to develop the high performance flash memories.

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Reference

[1]K. Naruke et al, IEDM, p424, 1988 [2]Y. Manabe et al, IEEE Trans. Semi. Manuf, p170, 1999 [3]Y. Kumagai et al, IRPS, p219, 2008 [4]R. Yamada et al, IRPS, p491, 2003

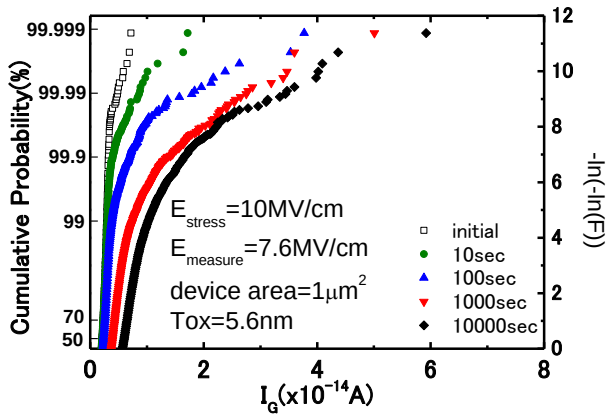

Fig.1. Distributions of gate leakage current of 87,344 MOSFETs at various stress time. The tail distribution of gate current increases with an increase of the stress time.

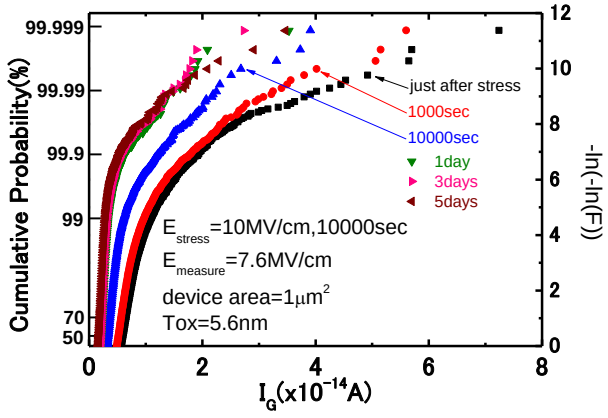

Fig.2. Distributions of gate leakage current of 87,344 MOSFETs measured after the stress for five days. The number of tail cells decreases with time increases after the stress.

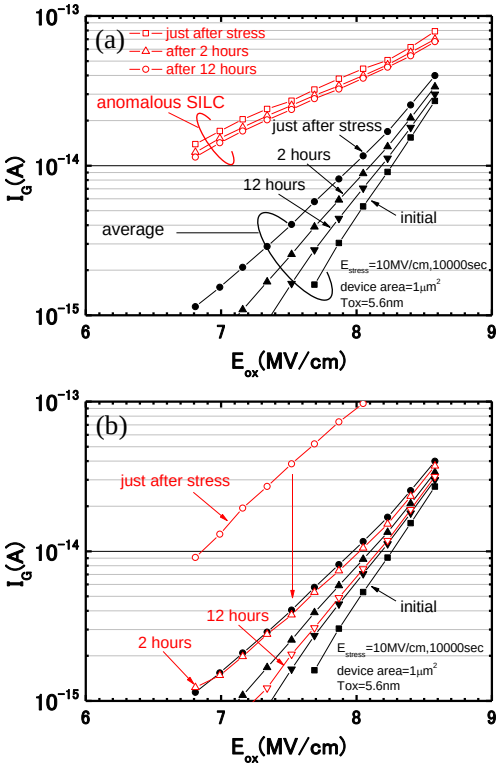

Fig.3. I_g-E_{ox} characteristics of anomalous SILCs and average SILCs. Average leakage current decreases with time after the stress. (a) The cell indicates anomalous SILC throughout the 12 hours. (b) The cell indicates the recovery characteristic.

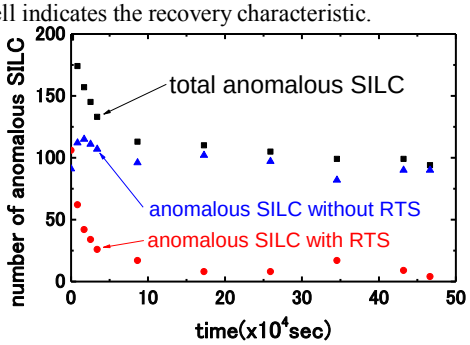

Fig.7. Number of anomalous SILCs after the stress for five days. After the recovery, the remained cells with RTS are less than those without RTS.

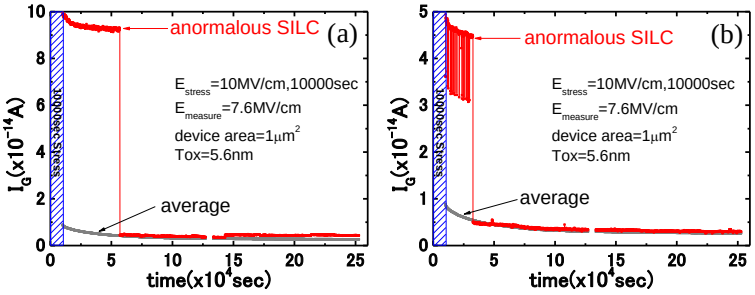

Fig.4. Transient characteristics of anomalous SILC. These cells showed recovery characteristics and suddenly changed to normal cells. (a) Anomalous SILC without RTS. (b) Anomalous SILC with RTS.

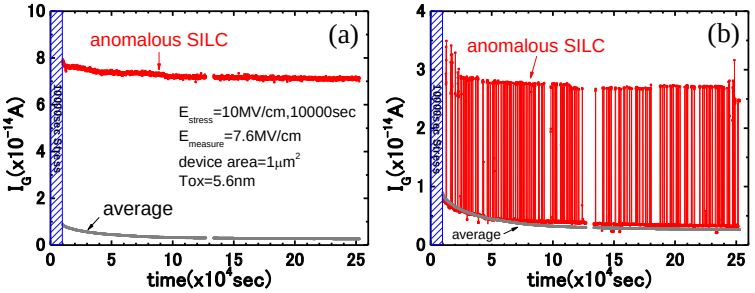

Fig.5. Transient characteristics of anomalous SILC which did not show recovery characteristic. (a) Anomalous SILC without RTS. (b) Anomalous SILC with RTS.

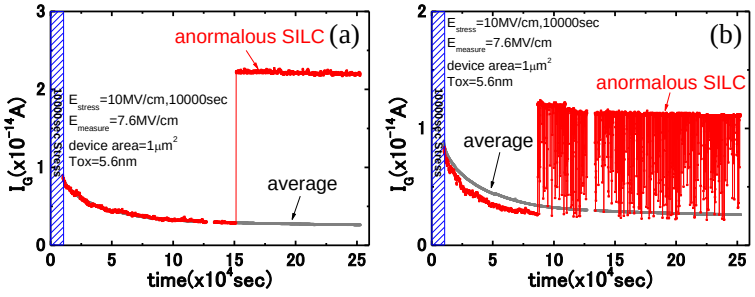

Fig.6. Transient characteristics of anomalous SILC. These cells showed generation characteristics and suddenly change to anomalous cells. (a) Anomalous SILC without RTS. (b) Anomalous SILC with RTS.