Tunnel Field-Effect Transistor with L-shaped Germanium Source: Device Physics and Design

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ABSTRACT

A novel Tunneling Field-Effect Transistor (TFET) with a L-shaped Ge source is investigated. The device comprises a Ge source that extends underneath a Si-channel region and separated from the drain by an insulator (SiO2). By optimizing the overlap length of the extended source L GS and the Si body thickness T Si, the current due to vertical band-to-band tunneling (BTBT) of the Ge-Si heterojunction could be increased significantly and is scalable with L GS. This leads to higher I DS and improved S. The SiO2 also reduces off-state current I OFF by reducing the drain coupling. With extensive simulation, the device physics and design guidelines of the novel structure are outlined.

INTRODUCTION

Tunneling Field-Effect Transistor (TFET) is a promising logic device that can achieve a high I ON/I OFF ratio for sub-0.5 V supply voltage V DD and significant reduction in power consumption [1]-[4]. The TFET operates on band-to-band tunneling BTBT and can achieve a sub-60 mV/decade subthreshold swing S at room temperature. However, TFET suffers from low drive current. Various works to alleviate this issue have been reported, including use of hetero-junction [5], multi-gate device architecture [6], bandgap engineering [7]-[8], and specially-designed source structures [9].

In this paper, an alternative novel structure with a L-shaped source for increased vertical tunneling region beneath the channel is proposed [Fig. 1(a)]. An insulator (SiO2) is positioned between the source and drain to reduce the drain coupling effect on the tunneling junction and to reduce I OFF. Extensive simulation study of the effects of overlap length and silicon thickness on the ON state current and sub-threshold swing of TFET is carried out. In addition, the physics and device design of the novel structure are explored in detail.

DEVICE STRUCTURE AND METHODOLOGY

The basic device structure comprises a single-gated Si-body TFET with Ge extended source as shown in Fig. 1. A SiO2 region is adjacent to the Ge extended source and beneath the drain region. A two-dimensional (2D) TCAD simulator with a physics-based non-local BTBT algorithm [10] was developed and used for this simulation. For all simulations, the device has a gate length of 50 nm and EOT of 0.8 nm. I ON is extracted at V GS = 0.4 V and V GS - V OFF = 0.4 V. V OFF is extracted at I DS = 10^-6 mA/μm. S is calculated as the average swing for I DS = 10^-9 mA/μm to 10^-3 mA/μm. Fig. 1(b) depicts the control device whereby L GS = 0.

RESULTS AND DISCUSSION

Simulated gate transfer characteristics with increasing L GS at T Si = 5 nm is shown in Fig. 2. Improved S and higher V TH are observed with progressively larger L GS. At L GS = 30 nm, S improves from 35.8 mV/dec to 8.4 mV/dec with V GS being 0.1 V higher. At fixed I OFF, I DS is also 20x higher [Fig. 2(b)]. The higher V TH could be explained by Fig. 3, which compares the band diagram along the source-to-drain direction, for the control device and a 30 nm-overlap device in OFF state and under bias condition of V GS = 0.4 V and V GS = 0.18 V. The existence of the overlap region increases the tunneling barrier width in the lateral direction [Fig. 3(b)]. Hence, a higher gate voltage is needed to reduce the tunneling width. Fig. 4 shows the trend of increased lateral tunneling width with increasing L GS. The higher I ON and steeper S for larger L GS are the result of increased number of vertical tunneling paths. For L GS = 0, the dominant current conducting path is lateral tunneling and it gets weaker further from the surface. For L GS = 30 nm, vertical tunneling is the main contribution to higher I ON. A more uniform BTBT in the vertical hetero-junction direction leads to initiation of tunneling from the Ge-Source to Si-body at a similar V GS in the tunneling region, resulting in steeper S. This is verified by the better uniformity of BTBT rate contour for the device with L GS = 30 nm compared to the control device at T Si = 5 nm (Fig. 5).

The impact of L GS on I ON for various T Si is illustrated in Fig. 6. I ON decreases with increasing T Si. This is caused by the weakening of gate coupling to the channel [11] due to thicker T Si. As such the BTBT generation rate of the device with thicker T Si of 10 nm is about 2 orders of magnitude lower than that in a device with thinner body (Fig. 7). S is lower for a larger L GS and a thinner T Si (Fig. 8), contributed by the better uniformity of BTBT along the vertical tunneling direction.

For device with L GS = 50 nm, the impact of L GS is less significant due to weak vertical tunneling when T Si is greater than 10 nm. For higher I ON and steeper S, T Si smaller than 8 nm and L GS greater 10 nm should be used.

CONCLUSION

A novel TFET with L-shaped Ge source is studied. The device physics and design is detailed through 2-D simulation. It is found that the source overlap region underneath the channel region improves I ON and S. This is due to the more dominant and uniform vertical tunneling from the Ge source to the Si channel. In order to achieve this, the Si channel needs to be thin enough for more effective gate-to-channel coupling. As such, I ON is scalable with L GS. This alleviates the I ON limitation and scalability issue faced by most lateral TFET design.

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REFERENCES

**Fig. 1.** (a) TFET structure with a L-shaped Ge source extended beneath the Si channel by an amount $L_{OV}$. (b) Control device with $L_{OV} = 0$.

**Fig. 2.** (a) $I_{DS}(V_{GS})$ and (b) $I_{DS}(V_{GSOFF})$ of TFET with various $L_{OV}$ and $T_S = 5$ nm. By increasing $L_{OV}$ from 0 to 30 nm, $S$ is improved by 27 mV/decade, $I_{ON}$ is enhanced by 20 times, and $V_{TH}$ is also higher by 0.1 V.

**Fig. 3.** Energy band diagram along source-to-drain of device with $T_S = 5$ nm for (a) $L_{OV} = 0$ nm, and (b) $L_{OV} = 30$ nm in OFF-state and biased at $V_{DS} = 0.4$ V and $V_{GSOFF} = 0.18$ V. The introduction of the overlap region in (b) increases the lateral tunneling barrier width encountered by the valence electrons in the source region.

**Fig. 4.** Energy band diagram along source-to-drain of device with $T_S = 5$ nm in OFF-state for $L_{OV} = 10$, 20, and 30 nm.

**Fig. 5.** BTBT Generation rate contour of device with $T_S = 5$ nm for (a) $L_{OV} = 0$ nm, and (b) $L_{OV} = 30$ nm. The better uniformity of BTBT rate distribution over the overlap region shown in (b) results in a concerted electron tunneling in the vertical direction at a certain $V_G$, giving rise to steeper $S$.

**Fig. 6.** $I_{ON}$-$T_S$ for $L_{OV} = 10$, 20, and 30 nm. $I_{ON}$ is a strong function of $L_{OV}$ at small $T_S$.

**Fig. 7.** BTBT Generation rate contour of device with $L_{OV} = 30$ nm for (a) $T_S = 5$ nm, and (b) $T_S = 10$ nm. Higher BTBT rate in 5 nm Si-body device is due to better gate electrostatic control over the vertical tunneling junction.

**Fig. 8.** $S$-$T_S$ for $L_{OV} = 10$, 20, and 30 nm. 3 times reduction in $S$ is obtained for $T_S = 5$ nm and $L_{OV} = 30$ nm.