Impact of Random Telegraph Noise Reduction with Buried Channel MOSFET

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1. Introduction
Random telegraph noise (RTN) has become one of the critical issues as CMOS processes scale down [1, 2]. RTN causes a phase noise increase of the oscillation circuit and the S/N ratio degradation in analog circuits. An image quality of CMOS imager is also degraded by RTN at the in-pixel source follower amplifier [3, 4]. It has been reported that using buried channel MOS transistor, dark random noise of CMOS image sensor is reduced [5]. In this work, we evaluate RTN of buried channel MOS transistor based on statistical measured data and investigate relationship between depth of buried layer and its effect to RTN characteristic, short channel effect and threshold voltage (\(V_{th}\)) variation.

2. Experimental
Fig. 1 shows the schematic illustration of the buried channel nMOS transistor and a depth profile of net dopant under gate insulator/silicon interface. To form the buried layer shown in Fig. 1, the ion implantation condition at the \(V_{th}\) adjustment process was modified for the transistors under evaluation with an additional photomask. In order to investigate the relationship between the depth of buried layer and its RTN reduction effect, we prepared four samples with different buried layer depth as shown in Table 1. To evaluate RTN, we used the test structure which can measure RTN for 1 million MOSFETs in a very short time (0.7s per 1 scan) reported in [6, 7]. The test structures were fabricated with a conventional 0.22\(\mu\)m CMOS logic process including thermal 5.7nm gate oxide, STI, and LDD.

3. Results and Discussions
Fig. 2 shows \(I_D-V_{G}\) characteristic of the buried channel and standard nMOS transistors. As the buried layer deepened, \(V_{th}\) drops to a lower value. Fig. 3 shows the distributions of RTN amplitude (\(V_{RMS}\)) which is defined by root mean square of gate-source voltage in the 300 times sampling (0.7s per 1 scan). In Fig. 4, the tail parts are reduced drastically as buried layer depth increases. This means noise intensity and occurrence frequency decreases effectively as the position of carrier conduction path becomes more away from the interface. In order to confirm that the carrier conduction path becomes more away from the gate insulator/silicon interface as buried layer deepened, gate-channel capacitance (\(C_{GC}\)), electron mobility (\(\mu_{eff}\)) and channel charge density (\(Q_{ch}\)) were evaluated. Fig. 4 shows \(C_{GC}-I_D\) characteristics of buried channel and standard transistors. When the same drain current is driven, \(C_{GC}\) of buried channel transistor is smaller than that of standard device. \(C_{GC}\) decreases so that the distance between the gate insulator/silicon interface and carrier conduction path is longer. Fig. 5 shows \(\mu_{eff}\) and \(Q_{ch}\) v.s. \(L_w\) for different buried layer depth. Because as buried layer deepened, the interface roughness scattering is effectively suppressed and the transverse electric field becomes weaker, than \(\mu_{eff}\) increases. \(Q_{ch}\) for same drain current is smaller in the buried channel transistors than that in standard transistor because of an increase in \(\mu_{eff}\). Back bias dependence of \(V_{RMS}\) distributions are shown in Fig. 6. Noise intensity increases with an increase in back bias. The career is pressed to the interface by the applied back bias as shown in the energy band diagram in Fig. 7. When the same drain current is driven, the \(\mu_{eff}\) decreases as applied back bias increases due to an increase of the electric field. Because of this, it can be considered that an increase in \(Q_{ch}\) density causes a decrease in RTN [8]. However, RTN increases actually by the applied back bias as shown in Fig. 6. These results suggest that the RTN intensity strongly depends on the distance between the interface and the carrier conduction path rather than the \(Q_{ch}\). Fig. 8 (a) and (b) show RTN amplitude as a function of drain current and gate area (LW), respectively. In these graphs, the \(V_{RMS}\) at cumulative probability of 99.99% are plotted. In Fig. 8, RTN decreases as \(I_D\) or gate area increases. Also, the values of \(V_{RMS}\) of the sample “Deep” are almost the same level as the floor noise level of the measurement system. Fig. 9 shows \(V_{th}\) roll-off characteristics of the buried channel and standard nMOS transistors. As buried layer deepened, roll-off characteristic becomes degraded. Fig. 8 shows distributions of \(V_{th}\) with 65536 transistors for each sample. Mean values of \(V_{th}\) decreases and as shown in Fig. 10, standard deviation of \(V_{th}\) \((\sigma_{Vth})\) increases with an increase in buried layer depth. The increase of \(\sigma_{Vth}\) is considered to be due to the decrease of \(C_{GC}\) at the measured \(I_D\) [9]. Fig. 12 shows output resistance \(R_{on}\) of each sample, \(R_{on}\) becomes smaller as buried layer deepened. These results offer the important parameters for the low noise analog circuit design with buried channel transistors.

4. Conclusions
A significant reduction of RTN is demonstrated by the buried channel transistor structure. It was revealed that the RTN intensity strongly depends on the distance between the gate insulator/silicon interface and carrier conduction path rather than the channel carrier density. As buried layer becomes deeper, \(V_{th}\) roll-off, \(V_{th}\) variation, and \(R_{on}\) are degraded. However, it is practically applicable according to the application of analog circuits, such as differential amplifiers and source followers. For instance, the \(V_{th}\) variation can be removed by the correlation double sampling in CMOS image sensor.

References
Table 1 Buried layer depth for prepared samples.

<table>
<thead>
<tr>
<th>Sample name</th>
<th>Buried layer depth [nm]</th>
</tr>
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<tbody>
<tr>
<td>Shallow</td>
<td>50</td>
</tr>
<tr>
<td>Middle</td>
<td>130</td>
</tr>
<tr>
<td>Deep</td>
<td>170</td>
</tr>
<tr>
<td>Standard device</td>
<td>-</td>
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Fig. 1 Schematic illustration of buried channel nMOS transistor.

Fig. 2 $I_D$-$V_G$ characteristics of the buried channel and standard nMOS transistors.

Fig. 3 Distributions of RTN amplitude ($V_{RMS}$) in Gumbel plot. Noise intensity and occurrence probability decreases drastically as the buried layer becomes deeper.

Fig. 4 $C_{GC}$-$I_D$ characteristics of buried channel and standard transistors. When the same drain current is driven, $C_{GC}$ of buried channel transistor is smaller than that of standard device.

Fig. 5 $I_D$ and $Q_s$ vs. $I_D$ for different buried layer depth. As buried layer deepened, electron mobility increase. Channel carrier density for the same drain current is smaller in the buried channel transistor because of an increase in mobility.

Fig. 6 Back bias dependence of $V_{RMS}$ distribution. Noise intensity increases with an increase of back bias.

Fig. 7 Energy band diagram with or without back bias. The career is pressed to the interface by the applied back bias applying. Therefore, the channel approaches closer to the interface.

Fig. 8 (a) $I_D$ and (b) gate area dependence of $V_{RMS}$ at cumulative probability of 99.99%.

Fig. 9 $V_{th}$ roll-off characteristics of the buried channel and standard nMOS transistors. As buried layer deepened, roll-off characteristic becomes more significant.

Fig. 10 Distributions of threshold voltage ($V_{th}$) with 65,536 transistors for each sample. Mean values of $V_{th}$ decreases and standard deviation of $V_{th}$ ($\sigma_{V_{th}}$) increases with an increase in buried layer depth.

Fig. 11 Standard deviation of $V_{th}$ vs. $1/\sqrt{LW}$ (Pelgromplot). The $\sigma_{V_{th}}$ increases in proportion to $1/\sqrt{LW}$ and the slope increases with the increase in buried layer depth. It is considered that for the buried channel devices, the smaller gate-channel capacitance and short channel effect results in the higher variation.

Fig. 12 Output resistance ($r_{oa}$) vs. gate length. $r_{oa}$ becomes smaller as buried layer becomes deeper.