Characteristics of hot hole injection, trapping, and detrapping in gate oxide of poly-Si TFTs

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1. Introduction
Poly-Si thin film transistors (TFTs) are not only widely used as switching devices in active-matrix displays, but also expected to realize more functional digital and analog circuits integrated on a glass substrate [1]. In this device, hysteresis behaviors are often observed, whose mechanisms have been attributed to the electron trapping/detrapping processes associated with the deep-level traps in the grain boundaries of the poly-Si channel [2], the hole trapping/detrapping into/from the gate oxide defects [3], etc. Though such phenomena are undesirable for circuit applications, by engineering the hysteresis mechanisms, nonvolatile memories have been proposed, e.g., SONOS type poly-Si TFT Flash memory using channel hot-electron (CHE) programming and band-to-band hot hole (HH) erasing [4].

In this work, in-depth investigation of hysteresis characteristics observed in the off-state leakage current in poly-Si TFTs is presented. We discuss on the mechanisms responsible for inducing the shift and the recovery of the transfer characteristics depending on the bias conditions. Moreover, the measurements are demonstrated to be useful to characterize the internal device parameters related to the thermal and the trap properties.

2. Experimental
In this study, n-channel poly-Si TFTs with a single drain structure fabricated on a glass substrate were used. The gate size was L/W = 4 μm/20 μm. The poly-Si active layer was formed by metal-induced crystallization with a thickness of 50 nm, while the gate oxide of 80 nm was deposited by plasma-enhanced CVD. The electric characteristics were measured on the temperature controlled stage in the range of 300 K–400 K.

3. Results and Discussion

Hysteresis Characteristics and Mechanism: Fig. 1 shows the $I_d-V_g$ characteristics of the poly-Si TFT. The gate voltage was repeatedly swept between $+15$ V and $-15$ V with a constant $V_d$. The hysteresis characteristics were clearly observed in the negative $V_g$ region under $V_d = 8$ V. It was confirmed that the same characteristics can be repeatedly obtained at least for 10 times up-and-down sweeps. To clarify the origin of the hysteresis behavior, constant voltages were applied to the fresh samples, followed by monitoring the $I_d-V_g$ characteristics with a low $V_d$ (Fig. 2). The results indicate that the application of the high negative $V_g$ and the positive $V_d$ reduces the off-leakage current in the TFT, suggesting the possible mechanism related to the HH injection into the gate oxide. As shown in Fig. 3, the holes created by band-to-band tunneling are accelerated by a high field and injected into the gate oxide near the drain edge, and the trapped holes shift the $I_d-V_g$ characteristics to the left [5]. Although $I_d(V_g > 0)$ is not sensitive to the localized positive charges, we have confirmed the threshold voltage shift under low $V_d$ or when source and drain terminals were reversed. The retention characteristics of the trapped holes are shown in Fig. 4.

Hole Detrapping: As shown in Fig. 1, the shift of $I_d-V_g$ characteristics induced during negative $V_g$ scan was fully recovered after positive $V_g$ scan, indicating the annihilation of the positive charges. This was verified by the experiment depicted in Figs. 5 and 6. Note that the bias conditions necessary to erase the trapped holes are well characterized by $I_d V_d > 9 \text{ mW}$, suggesting the strong correlation with the self-heating mechanism [6] as shown in Fig. 7 (not the charge compensation by CHE injection). We have also confirmed that when the sample was put on the hot stage, the threshold power $P = I_d V_d$ required for the erase operation was decreased (Fig. 8), whose characteristics are plotted in Fig. 9 as a function of the stage temperature $T_0$. The fitting to the thermal equivalent circuit model [7] gives the thermal resistance between the device and the stage as $R_{th} = 1.6 \times 10^4$ K/W, which is a reasonable order of magnitude for the TFTs fabricated on a glass substrate [8]. The thermal analysis also gives the estimation of the device temperature $T$ required for the hole detrapping. Considering the thermal activation, the inverse of the hole detrapping time constant is given by

$$
\tau^{-1} = a T^2 \exp \left( - \frac{E_t}{k_B T} \right),
$$

where $a = 3 \times 10^8 \text{ K}^{-2} \text{sec}^{-1}$ [9] and $E_t$ is the trap level measured from the top of the SiO$_2$ valence band edge. If we substitute $\tau = 10 \text{ s}$ and $T = 450 \text{ K}$ (from Fig. 9), then $E_t \sim 1.3 \text{ eV}$ is obtained, which is slightly less than the value reported for the thermally grown SiO$_2$ films (peak $\sim 1.8 \text{ eV}$ [9]).

4. Conclusions
The hysteresis observed in the n-poly-Si TFTs have been investigated, and the mechanisms have been discussed. The localized positive charges built up by band-to-band HH injection were erased by self-heating, which is particularly pronounced in the TFT structures due to the worse thermal conductance through the thick glass substrate. These processes provide information inside the TFT ($R_{th}$ and $E_t$), and also might be utilized as another write/erase scheme for the nonvolatile memory.
Fig. 1 Measured $I_d$-$V_d$ characteristics of n-ch TFT biased with $V_d = 8$ V (solid line) and 1 V (dashed line). $V_g$ was swept repeatedly between $-15$ V and $+15$ V with a sweep rate of $\sim 1$ V/sec.

Fig. 2 $I_d$-$V_d$ characteristics measured with $V_d = 1$ V after applying various stress voltages ($V_d = 8$ V and $V_g = -5$, $-10$, $-15$ V) for 10 sec (symbols). The data for the sample without stress is also shown for comparison (line).

Fig. 3 Mechanism for the hole detrapping at the drain edge during the off-state condition under high $V_d$. Holes generated due to band-to-band tunneling are accelerated by the electric field, and part of them could be thermally injected into the gate oxide layer.

Fig. 4 Time evolution of $I_d$ measured with $V_d = 3$ V and $V_g = 0.1$ V after injecting hot holes at the drain side junction with $V_d = 8$ V and $V_g = -20$ V for 10 sec (solid line). The current of the fresh sample is plotted with dashed line for comparison.

Fig. 5 Measurement results examining the hole detrapping during the on-current conduction. Firstly, $I_d$-$V_d$ characteristics were measured by sweeping $V_g$ from 0 V to $-15$ V (line). Then constant bias with (i) $V_d = 8$ V and $V_g = 15$ V or (ii) $V_d = 8$ V and $V_g = 10$ V was applied for 10 sec. Finally, $I_d$-$V_d$ characteristics were measured again (symbols).

Fig. 6 The conditions required for erasing the trapped holes in the gate oxide. After injecting holes, various constant biases ($V_d = 6$ V $\sim 10$ V, $V_g = 8$ V $\sim 15$ V) were applied for 10 sec. The open circles and the crosses indicate the conditions when the hole annihilation was confirmed or not, respectively. The solid curve indicates $I_dV_d = 9$ mW.

Fig. 7 Mechanism for the hole detrapping at the drain edge during the on-state condition. The temperature in the poly-Si body region is raised due to the self-heating effect, which enhances the thermal emission of holes trapped in the oxide layer.

Fig. 8 Boundaries for the bias conditions required to erase the trapped holes (see, Fig. 6) measured at various stage temperatures ranging from 300 K to 400 K. The lines are the fitted curves indicating constant input power $P = I_dV_d$.

Fig. 9 Input power $P = I_dV_d$ required to erase the trapped holes plotted as a function of the stage temperature $T_0$. The experimental data (symbols) are fitted to the characteristics given by the thermal equivalent circuit model (line).

References