Extremely Small Within-Device Variability in Intrinsic Channel Tri-Gate Silicon Nanowire MOSFETs

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1. Introduction

Along with the device scaling, the variability turns to be one of the major concerns [1]. It is known that random dopant fluctuation (RDF) is the dominant origin of random $V_{TH}$ variability in conventional bulk MOSFETs [2]. It is reported that the variability of both DIBL (drain induced barrier lowering) and $COV$ (current-on-set voltage) is also caused by RDF [3-5] and leads to instability of SRAM cells [6] and drain-current variability [3].

Recently, we have shown that intrinsic channel fully depleted (FD) SOI MOSFETs have not only smaller $V_{TH}$ variability but also smaller DIBL and $COV$ variability thanks to the absence of RDF [7]. However, the DIBL and $COV$ variability still remains possibly due to variability of workfunction in metal gate electrode, and further reduction of variability is strongly required for better circuit performance variability and SRAM stability.

In this work, within-device variability of $V_{TH}$, DIBL and $COV$ in intrinsic channel silicon nanowire MOSFETs was evaluated and compared with conventional bulk and FD SOI MOSFETs. It is found that within-device variability of DIBL and $COV$ as well as $V_{TH}$ is extremely small in intrinsic channel nanowire MOSFETs.

2. Experiment Method

Intrinsic channel tri-gate silicon nanowire nFETs with [110] channel direction were fabricated on (001) SOI wafers with a 24nm thick SOI film [8]. Polycrystalline Si gate and 4nm SiO$_2$ are used as gate stacks. No impurities are intentionally doped into the channel region. Raised S/D with 25nm-thick epi-Si is employed to reduce S/D resistance.

The nanowire width $W_{NW}$ is 30nm, and nanowire length $L_{NW}$ is varied. Fig. 1 shows $I_{DS}$-$V_{GS}$ characteristics of 18 nanowire nFETs in a wafer. $V_{TH}$ is evaluated with two definitions: $V_{TH}$ and $V_{THC}$. $V_{TH}$ is defined by subthreshold constant current ($I_{DS}=10^{-8} \times W/L$) and $V_{THC}$ is extrapolated $V_{TH}$ ($V_{GS}$ intercept of tangent line with largest slope in $I_{DS}$-$V_{GS}$).

Since the number of measured FETs with the same size is only 18 and the measured variability may include a systematic component, “within-device” variability (difference between forward and reverse device by exchanging S/D) [9] is mainly evaluated in order to examine intrinsic variability of devices.

3. Results and discussion

Figs. 2 and 3 show $V_{THC}$ variability in linear region in Pelgrom plot and cumulative plot, respectively. Compared with bulk nFETs ($A_{VF}=4.25$) and SOI nFETs ($A_{VF}=1.36$), a clear variability suppression can be seen in nanowire nFETs. The slope $A_{VF}=0.71$ is close to the “universal line” of $A_{VF}=0.6$ reported in Ref. [10], indicating that the systematic component is small enough and the present variability data are validated.

Fig. 4 shows $V_{THC}$ variability in saturation region. Smaller $A_{VF}$ is seen in nanowire FETs. It should be noted that more variability suppression in nanowire FETs is obtained in Figs. 5 and 6 in “within-device” variability, $\sigma\Delta V_{THC}$, where $\Delta V_{THC} = V_{THFORward} - V_{THREVERSE}$ measured by S/D exchange. Fig. 5 shows extremely small $\sigma\Delta V_{THC}$ in nanowire FETs. This is because a wafer-level systematic component is completely suppressed in within-device variability in Fig. 5. The good normal distribution of nanowire nFETs in cumulative plot of $\Delta V_{THC}$ (Fig. 6) also confirms the great suppression.

DIBL variability is compared in Figs. 7-9. The Pelgrom plot in Fig. 7 shows smaller $A_{VF}$ in nanowire FETs. In particular, the within-device variability of DIBL ($\sigma\Delta DIBL$) (Fig. 8) is extremely small in nanowire FETs. Fig. 9 is cumulative plot of $\Delta DIBL$, which confirms the suppression in nanowire nFETs once again.

$COV$ is defined as $COV = V_{THEX} - V_{THC}$ [3]. Fig. 10 shows Pelgrom plot ($\sigma COV$) and Fig. 11 shows within-device variability ($\sigma\Delta COV$). Fig. 12 is cumulative plot of $\Delta COV$. Again, within-device $COV$ variability is extremely small in nanowire FETs compared with bulk and SOI FETs.

The remaining variability in FD SOI FETs is caused by the workfunction variability in metal gate. In the present nanowire FETs, the workfunction variability is negligible by using poly-Si gate. The measured data above indicate that the negligible small $V_{TH}$, DIBL and $COV$ variability can be achieved as long as the workfunction variability is completely suppressed.

4. Conclusions

It is experimentally found that within-device variability of not only $V_{TH}$ but DIBL and $COV$ is suppressed in intrinsic channel nanowire FETs thanks to non-intentionally doped channel and absence of gate workfunction variability.

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References

Fig. 1. Measured $I_{ds}-V_{ds}$ of 18 NW-NFETs.

Fig. 2. Pelgrom Plot of $\sigma V_{THX}$.

Fig. 3. Cumulative distribution of $V_{THX}$.

Fig. 4. Pelgrom Plot of $\sigma V_{THC}$.

Fig. 5. Pelgrom Plot of within-device $\sigma V_{THC}$.

Fig. 6. Cumulative distribution of $\Delta V_{THC}$.

Fig. 7. Pelgrom Plot of $\sigma DIBL$.

Fig. 8. Pelgrom Plot of within-device $\sigma DIBL$.

Fig. 9. Cumulative distribution of $\Delta DIBL$.

Fig. 10. Pelgrom Plot of $\sigma COV$.

Fig. 11. Pelgrom Plot of within-device $\sigma COV$.

Fig. 12. Cumulative distribution of $\Delta COV$. 