Advantages of Silicon Nanowire MOSFETs over Planar Ones Investigated from the Viewpoints of Static and Noise Properties

W. Feng1,2, R. Hettiarachchi1,2, S. Sato3, K. Kakushima3, M. Niwa1,2, H. Iwai1, K. Yamada1,2, K. Ohmori1,2

1Graduate School of Pure and Applied Sciences, University of Tsukuba, I-1-1 Tennodai, Tsukuba, Ibaraki 305-8573, Japan
2JST-CREST, 3Tokyo Institute of Technology

Phone: +81-29-849-1575, Fax: +81-29-849-1533, E-mail: feng wei ft u tsukuba ac

1. Introduction

A silicon nanowire MOSFET (SNWFET) is considered as one of the promising candidates to extend the downsizing of CMOS technology beyond FInFETs, due to the excellent gate controllability, high drain-current drivability, quasi-ballistic transport properties, and CMOS compatibility [1].

The influence of low-frequency noise (LFN) on the circuit performance is well known as one of the most pronounced issues with technology downsizing.

In this paper, we present our study on dynamic noise fluctuation of SNWFETs, which exhibits an excellent static property and a quiet noise power density at the same time.

2. Device fabrication and measurements

N-type SNWFETs were fabricated on <110>-oriented silicon-on-insulator (SOI) wafers. The details of processes are described elsewhere [2]. Figure 1(a) shows an SEM image of the fabricated SNWFET. The cross-sectional size of SNWFETs is about 17 and 12 nm for width and height, respectively, resulting in a perimeter of 42 nm (Fig. 1(b)). For comparison, planar MOSFETs with a gate width of 2.5 µm were employed. The oxide thickness for planar MOSFETs is 3.2 nm, while we estimated the average thickness for SNWFET as 3.8 nm. The oxidation condition for both FET types is same. We attribute this to the 3D structure of SNWFET because it contains (110) planes along the sides, on which the oxidation rate is faster than (001). SNWFETs with multi (64) channels, which are equivalent to 2.6 µm in the total gate width, were used in order to make a fair comparison with the planar ones.

Static properties were measured using a conventional semiconductor device analyzer, while for acquiring power spectral densities of drain-current noise (SdId), Agilent B1530A (fast I-V) unit was carried out. Sampling rates from 1 ksp (samples per second) to 1 Msps were used. The gate overdrive (Vg-Vt) was varied from -0.2 V to 0.6 V (every 0.1 V step) with a drain voltage Vd of 50mV. More than three FETs for each parameter (FET type, gate length (Lg)) were measured.

3. Results and Discussion

Figure 2 shows I d -V d characteristics of (a) SNWFET and (b) planar FET with gate lengths of 200 nm and 210 nm, respectively.

From static measurements, it is evident that the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) improve with increasing the gate length for both planar devices and the SNWFET (Fig. 3), resulting from lessening of short-channel effects (SCEs).

For both SS and DIBL coefficients, the SNWFET has smaller values comparing with the planar devices, which demonstrates a better electrostatic controllability in SNWFET.

This result confirms excellent SCEs immunity of the gate-around Si nanowire structure, being consistent with the previous reports [3,4].

The normalized drain-current noise spectral density SdId2 for SNWFET is shown in Fig. 4 demonstrating straight 1/f property. The SdId2 values at 100 Hz were extracted for further comparison between the SNWFETs and planar FETs.

The power spectral density normalized by Id and gate width is shown as a function of Id in Fig. 5. One of the factors that influences on this properties is the origin of noise such as number and mobility fluctuations [1]. We emphasize that the normalized SdId values for SNWFETs are lower than those for planar ones specifically in the Id ranges from 10−8 to 10−6 (A).

In general, the nicer property in SCE increases the noise intensity in the subthreshold regime because the diffusion current is predominant [5]. The total gate width of SNWFET (2.6 µm) is similar as that of planar one (2.5 µm). The normalized SdId value is expressed as

\[ \frac{S_{dI_d}}{I_{d}^{2}} = \frac{g_{m}^{2} KT q^{2} N_{st}}{I_{d}^{2} W L C_{ox}^{2}} \]  \hspace{1cm} (Eq. 1)

where a thicker oxide (smaller Cox) increases the value of SdId/Id [6].

Although further investigations on interface trap density is necessary, if the 3D structure of SNWFET results in larger trap density in the oxide [7], it usually increases the noise intensity.

Nevertheless, the normalized SdId exhibits better property than that of planar one. One of the possible reasons is that the position of charge-centroids in the channel is further from the interface in SNWFETs because of electrostatic effect due to the semi-gate around structure.

Ioff-Ioff Characteristic is shown in Fig. 6. The Ioff is defined as Ioff at Vg-Vt = -0.2 V, whereas Ion is evaluated at Vg-Vt = +0.8 V for Vd = 1 V. A SNWFET shows more excellent Ioff-Ioff property than a planar FET as previously reported [8,9].

4. Conclusion

We have experimentally demonstrated for the first time the advantages of Si nanowire FETs in noise properties by comparing with planar FETs of similar gate stack structures. Despite of thicker gate oxide, SNWFETs investigated in this work shows better Ioff-Ioff characteristics along with excellent electrostatic controllability, in addition to a lower noise density level, strongly suggesting the potentiality of the SNWFET.

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References
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Fig. 1 (a) SEM image of SNWFET after poly-Si gate etching. SNWFETs with 64 channels were used in order to avoid appearance of random telegraph signals as well as to make fair comparison with planar FET on the total gate width. The horizontal field of view is 3 µm. (b) Cross-sectional TEM image of nanowire channel. The gate oxide of the sides is thicker than that of the top by a factor of about 1.3, probably due to faster oxidation rate on a (110) plane.

Fig. 2 $I_d$-$V_g$ properties of (a) SNWFET and (b) planar FET (b), with $L_g = 200$ and 210 nm, respectively. Nanowire shows an excellent $I_d$-$V_g$ curve and better electrostatic controllability at the subthreshold region.

Fig. 3 (a) Subthreshold swing and (b) DIBL values as a function of gate length. SNWFET demonstrates lower values for both subthreshold swing and DIBL coefficients, which indicates a better electrostatic controllability.

Fig. 4 Noise spectral density of SNWFET, demonstrating straight $1/f$ property due to 64 multi-channels. The noise intensity decreases as the gate overdrive increases. The $S_{Th}/I_d^2$ values at 100 Hz were extracted for further discussion.

Fig. 5 Normalized noise spectral density $S_{Th}/I_d^2$ as a function of $I_d$. SNWFET exhibits lower noise density than planar one. One of the possible reasons could be that the position of charge-centroids in the channel is further from the interface.

Fig. 6 $I_{on}$-$I_{off}$ characteristics of SNWFET and planar FET. In order to compare performance between devices of different $V_t$, $I_{on}$ and $I_{off}$ were defined as $I_d$ at $V_g-V_t = +0.8$ and -0.2 V, respectively ($V_d = 1$ V). SNWFET shows more excellent $I_{on}$-$I_{off}$ property than planar FET.