HCI and NBII Induced statistical Variability in CMOS Transistors

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Abstract—This work studies the aging impact on CMOS transistors variability under NBII and HCI stress. Both the NBII and HCI contributions to random statistical variability are quantified as a function of device drift and compared to initial intrinsic one. The role of device geometries and oxide thickness are both investigated. In addition, the wafer level component of aging-induced variability is analyzed and compared to random local one.

I. INTRODUCTION

Statistical induced variability is one of the key concerns for modern CMOS technologies. It indeed induces serious limitations for both analog and digital applications such as SRAM that require highly reproducible threshold voltages. Since NBII and HCI mechanisms are spread (traps number and position over time randomly fluctuate from device to device) they are expected to significantly contribute to the overall variability as devices age. For NBII, assuming that the number of traps generated over time follows a Poisson distribution could provide a good fit with experiments over a wide range of oxide thickness and dimensions [1]. This model has been confirmed for several other technologies and transistor types [2][3]. More recently, “atomistic” simulations dedicated to the role of NBII on device intrinsic variability showed a good agreement with experiments [4]. However the HCI induced variability, despite reported to increase mismatch [5], has never been studied in details especially in terms of drift and dimension dependency. In this study, we first investigate the role of both NBII and HCI on statistical variability in order to quantify both theses aging contributions and their weight on overall variability, as a function of the device drift, dimensions and oxide thickness. Then, we show that, in addition to the random local variability there is also a wafer level component to the aging induced variability.

II. EXPERIMENTAL SETUP

The devices under study are N and PMOS transistors with a 18Å oxide dedicated to low power applications and a 9/0.65µm PFET transistor dedicated to high voltage applications with a 150A oxide. The test structures used in this study are matching test structures, which allow catching both the local random variability and the wafer level one since they were measured on full mappings. Fifty paired devices were measured, which allows limiting the sampling induced error. The P-FET devices were stressed under NBII (AC stress at 125°C), N and P FET were stressed under HCI (Vg=Vdd at 25°C/125°C for respectively N/P FET). Measurements were conducted prior and during stress.

III. RESULTS AND DISCUSSION

A. NBII induced mismatch

Figure 1 shows typical spreading of paired devices ΔVt distributions for different drift level under a HCI stress. It can be noted that the systematic mismatch (ΔVt average) remains null and, based on the 50 devices sample, no evidence of non Gaussian distribution can be claimed.

\[
\sigma_{\Delta Vt} = \sqrt{\frac{k}{Cox}} \cdot \frac{T_{average}}{2}, \quad n = 1/2
\]

In this study, the NBII-induced mismatch perfectly scales with the device dimensions. Fitting the normalized NBII-induced mismatch (\(\sigma_{\Delta Vt} \cdot W/L\)) with a power law of the average drift (ΔVt) leads to power factor values that are consistent with the expected ½ value and k constant values that are in the same order of magnitude of those reported by [1-3].

B. HCI induced mismatch

The HCI induced mismatch (for the stress conditions used in this study) is also found to follow a power law of the average drift. Both the power factor and the k factor are found similar to
the NBTI case (Figure 3). The difference between N and P is not clear and more devices are necessary to draw a conclusion. Both N and P perfectly scale in W. The power dependence keeps close to $\frac{1}{2}$ whereas k factor seems slightly above. Notice that only two device lengths were tested and additional tests are in progress to study deeper the L effect. Finally, it should be reminded that contrary to NBTI stress that provides straight forward correlation between VT and linear parameter. HCI stress leads to complex drift and stress dependent correlations (Figure 3 (b)). Consequently, on linear parameter, whereas results are expected to be similar in the NBTI case, they are expected to be significantly different and stress dependent in the HCI case.

\[ A_{\text{age}} = \sqrt{|k_{\text{age}}| \frac{q}{N_{\text{ox}}}} \]  

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Since the range of Vt degradation that will be allowed by technologies increases with oxide thickness, it is more pertinent to consider an oxide thickness normalized Vt shift ($\delta$=k.tox, $\delta$ in mV.A$^{-1}$). Also we remind that the mismatch is at first order linearly dependent on the oxide thickness [6] ($A_{w}$=k.tox). Then it appears that $A_{\text{age}}$ is not dependent on tox:

\[ A_{\text{age}} = \frac{\sqrt{k_{\text{age}}}}{\sqrt{k_{\text{tox}}}} \]  

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Since no correlation between the initial parameters and their drift was found, the total mismatch at a given a drift $A_{o}$ is the summation of initial mismatch ($A_{o}$) and the aging (NBTI or HCI) induced mismatch ($A_{\text{age}}$) (4) and the mismatch relative increase is given in (5).

\[ A_{\delta} = A_{o}^2 + A_{\text{age}}^2 \]  

\[ \frac{A_{\delta} - A_{o}}{A_{o}} = 1 - q(1 + \gamma + \beta) = \frac{\gamma^2 \beta}{2} \]  

Gamma depends only on $k$ which has been several times found close to 2 and $\alpha$ that is commonly reported close to 1. In order to get the range of magnitude the mismatch increase should be expected, we assume k=2 and $\alpha$ in the 0.8-1.2 mV.$\mu$m $\AA^{-1}$. The mismatch increase is given in Figure 4. The device "end of life" is of course a technological choice, but 3-5 mV/A is a reasonable value. This gives mismatch increase to be expected in the 20-55% range. For our specific experiments, the increase after 50mV/300mV drift for thin/thick oxide is reported in the table of Figure 4 for comparison to the theoretical expectation.

**D. Random local variability vs. wafer level variability**

Variability it is well known to contain a wafer level component, which weight increases in the overall mismatch when the device area increases (because local intrinsic component decreases) [7]. Interestingly, the aging-induced variability shows a similar behavior: neighbor devices (not necessarily electrically matched) age in a much more "mismatched" way than non-neighbor devices. Mathematically, this translates with the increase of the correlation between drift of paired devices with device area. For instance, in the NBTI case, it rises up to 66/88 for 5/25$\mu$m device (at 50mV drift). Practically this means that usage of paired devices, in addition to providing better initial matching, reduces the aging contribution. Moreover, because this correlation increases as the device drifts an important consequence for those large devices is that, considering the wafer-level aging-induced variability is very inaccurate (pessimistic) for predicting random local variability as a function of device drift (Figure 3).

**IV. SUMMARY**

We showed that the threshold voltage statistical variability induced by NBTI and HCI follows the same drift dependence. For NBTI we showed that the relative mismatch increase is independent of both dimension and oxide thickness. We finally evidenced that aging variability has an intrinsic and a wafer level component, introducing the notion of aging mismatch.

**REFERENCES**