Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp889-890

High-Electron-Mobility Ge n-MOSFET with TiN Metal Gate

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1. Introduction

Ge is of great interest as a candidate channel material for fabricating future CMOS devices due to its high intrinsic carrier mobility. To translate this potential into CMOS devices, a gate-stack with a high-quality interface is essential. One of the attractive interface passivation methods is to grow GeO_2, which is supposed to be a candidate interlayer (IL) between a gate-insulating film and a Ge substrate.

However, GeO_2 is difficult to integrate into the MOS fabrication process owing to its poor thermal stability and solubility in water. As a good method for solving this problem, our group has proposed the electrical passivation of a Ge surface by an ultrathin SiO_2/GeO_2 bilayer and achieved high-quality interface.[1)] Furthermore, we found that the interface state density (D_{it}) near the midgap could be decreased from 4×10^{11} to 1×10^{11} $cm^{-2}eV^{-1}$ by combining the bilayer passivation (BLP) with Al postmetallization annealing (Al-PMA).[2)] By using these techniques, we fabricated n- and p-MOSFETs on Ge (100) substrates and demonstrated the high electron and hole mobilities of 1097 and 376 $cm^2V^{-1}s^{-1}$, respectively.[3)]

Very recently, our group established TiN-gate Ge MOS fabrication process and investigated the PMA effect. As a result, the PMA at 450°C led to the incorporation of nitrogen atoms into the gate stack, which effectively terminated defects at the SiO_2/GeO_2 interface and/or in the GeO_2 IL.[4)] Thus, the TiN-gate Ge MOSFET with PMA at 450°C can be expected to enhance the channel mobility.

In this study, we established Ge n-MOSFET fabrication process with a TiN metal gate and investigated the device performance, which showed a high peak electron mobility of 1120 $cm^2V^{-1}s^{-1}$.

2. Experimental

We fabricated n-MOSFET using the gate-last process. The substrate used in this study was p-type (100) Ge with a resistivity of 0.35 Ωcm, corresponding to a substrate impurity concentration of 1×10^{16} cm^{-3}. Figures 1(a) and 1(b) show the fabrication process of n^+/p junctions for a source/drain (S/D) on the Ge substrate, and the details are given in Ref. 3.

The gate stack was fabricated using the BLP and subsequent SiO_2-gate insulator fabrication. The details are also given in Ref. 3. The postdeposition annealing (PDA) was carried out at 550°C for 30 min in N_2. Note that the physical thickness of GeO_2 was approximately 2 nm after the PDA.[2)] A 50-nm-thick TiN was deposited by rf sputtering using a TiN target in Ar ambient. Then, TiN gate electrode area was determined by the patterned photoresist and subsequent wet etching, as shown in Fig. 1(c), followed by PMA at 450°C for 20min in N_2.[4)]

As a final processing shown in Fig. 1(d), contacts holes were opened on the S/D region, and Al/TiN electrodes were formed on S/D contacts and gate electrodes by the lift-off process. Then, contact annealing was carried out at 350°C for 10 min in N_2. The reason for the use of TiN contact is to form the low contact resistance to n^+ S/D regions.[5)] The EOT (equivalent oxide thickness) of a MOS capacitor in the fabricated n-devices was 42 nm.

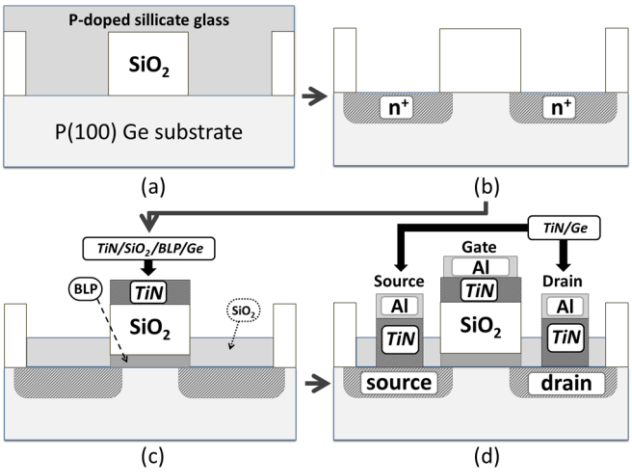

Fig. 1. Schematic process flow for n-MOSFET fabrication.

3. Result and Discussion

The current-voltage (I-V) characteristic of the fabricated n^+/p junction is shown Fig. 2, which indicates that a high On/Off ratio of 1.1×10^5 and an ideality factor of n = 1.1 were achieved. However, the leakage current of the junction with TiN contact is somewhat higher than that with Al.[3)] This is maybe due to damage during TiN deposition, because the deposition was performed using stronger power of 100 W.

Figure 3 shows the drain current (I_d) vs drain voltage (V_d) characteristics, where the threshold voltage (V_t) was 0.34 V. The result suggests successful operation of TiN-gate n-MOSFET.

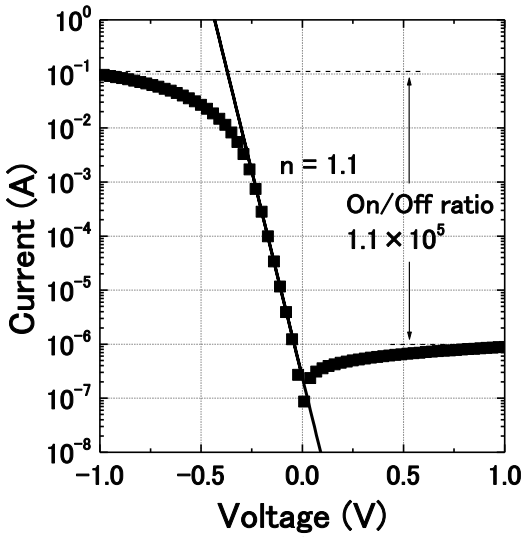

Fig. 2. *I-V* characteristic of Ge n^+/p diode. The junction area of the diode was 170 × 400 μm^2.

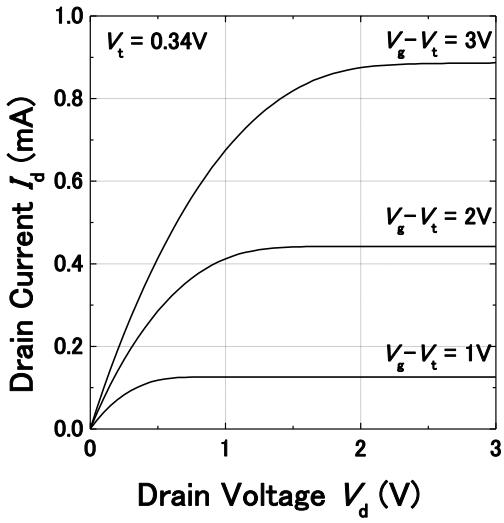

Fig. 3. I_d - V_d characteristics for Ge n-MOSFET. The channel length and width of MOSFET was 60 and 400 μm^2.

Figure 4 shows the source current (I_s) and I_d vs gate voltage (V_g) characteristics with V_d of 0.01 and 1 V. The values of I_d were almost the same as leakage currents of S/D junction shown in Fig. 2, implying that I_d under Off state is governed by the leakage current of S/D junction. Thus, I_s is real channel current. On/Off ratio of I_s was approximately 5×10^3 and 1×10^4 at V_d's of 0.01 and 1 V, respectively, which are almost the same as our previous study.[3)]

From I_s-V_g and split-*CV* measurements, the electron mobility was calculated as a function of inversion carrier density (N_s), as shown in Fig. 5, in which the result without PMA is also shown for a comparison. The peak mobilities with and without PMA were 1124 and 975 cm^{2}V^{-1}s^{-1}, respectively, which are approximately 1.8 and 1.5 times higher than that of Si n-MOSFET. The mobility for n-MOSFET with PMA shows large mobility enhancement in the low N_s range compared with that without PMA. These results suggest that PMA at 450°C was effective for decreasing D_{it} so that Coulomb scattering becomes weak in the low N_s region, which is consistent with the results in Ref. 4.

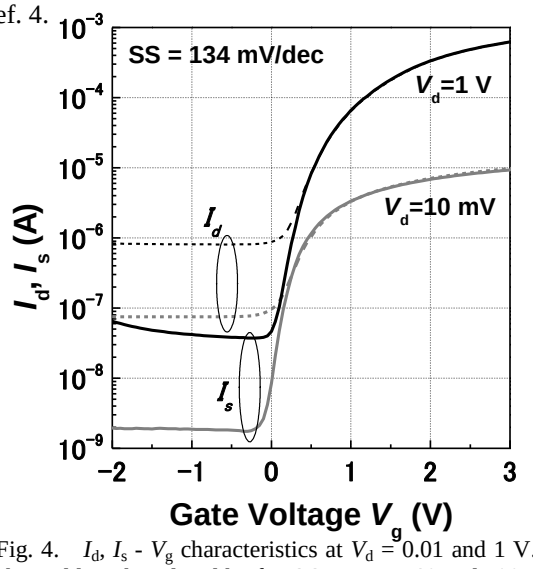

Fig. 4. I_d, I_s - V_g characteristics at V_d = 0.01 and 1 V. The channel length and width of MOSFET was 60 and 400 μm^2.

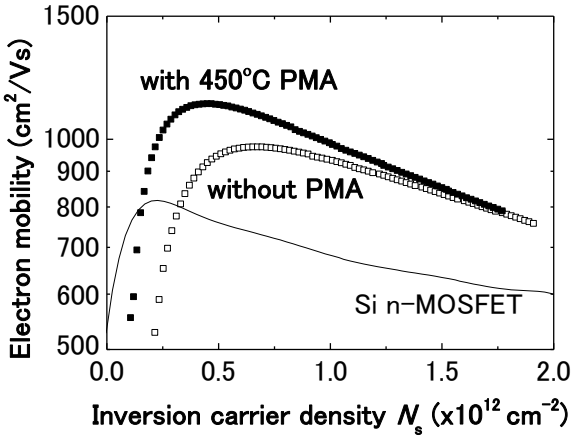

Fig. 5. Electron mobility versus N_s characteristics of Ge n-MOSFETs. The channel length and width of MOSFET was 40 and 400 μm^2. For comparison, the electron mobility of Si n-MOSFET is also shown.[6)]

4. Conclusion

TiN-gate n-MOSFET was fabricated on (100) Ge substrate using the gate last process. The MOSFET showed high On/Off ratio of over 10^5, and the peak electron mobility was 1120 cm^{2}V^{-1}s^{-1}. This fact comes from effective termination of defects at the SiO_2/GeO_2 interface and/or in the GeO_2 IL.

Acknowledgements

This study was partly supported by a Grant-in-Aid for Scientific Research from the MEXT in Japan.

References

1) K. Hirayama et al., Solid-State Electron. **60** (2011) 122.
2) K. Hirayama et al., Jpn. J. Appl. Phys. **50** (2011) 04DA10.
3) K. Yamamoto et al., Appl. Phys. Express **4** (2011) 051301.
4) H. Nakashima et al., Appl. Phys. Lett., to be published.
5) M. Iyota et al., Appl. Phys. Lett. **98** (2011) 192108.
6) K. Morii et al., IEEE Electron Device Lett. **31** (2010) 1092.