High-Electron-Mobility Ge n-MOSFET with TiN Metal Gate

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1. Introduction

Ge is of great interest as a candidate channel material for fabricating future CMOS devices due to its high intrinsic carrier mobility. To translate this potential into CMOS devices, a gate-stack with a high-quality interface is essential. One of the attractive interface passivation methods is to grow GeO₂, which is supposed to be a candidate interlayer (IL) between a gate-insulating film and a Ge substrate.

However, GeO₂ is difficult to integrate into the MOS fabrication process owing to its poor thermal stability and solubility in water. As a good method for solving this problem, our group has proposed the electrical passivation of a Ge surface by an ultrathin SiO₂/GeO₂ bilayer and achieved high-quality interface.3) Furthermore, we found that the interface state density (Dₙ) near the midgap could be decreased from 4×10¹¹ to 1×10¹⁰ cm⁻²eV⁻¹ by combining the bilayer passivation (BLP) with Al postmetallization annealing (Al-PMA).2) By using these techniques, we fabricated n- and p-MOSFETs on Ge (100) substrates and demonstrated the high electron and hole mobilities of 1097 and 376 cm²V⁻¹s⁻¹, respectively.3)

Very recently, our group established TiN-gate Ge MOS fabrication process and investigated the PMA effect. As a result, the PMA at 450°C led to the incorporation of nitrogen atoms into the gate stack, which effectively terminated defects at the SiO₂/GeO₂ interface and/or in the GeO₂ IL.3) Thus, the TiN-gate Ge MOSFET with PMA at 450°C can be expected to enhance the channel mobility.

In this study, we established Ge n-MOSFET fabrication process with a TiN metal gate and investigated the device performance, which showed a high peak electron mobility of 1120 cm²V⁻¹s⁻¹.

2. Experimental

We fabricated n-MOSFET using the gate-last process. The substrate used in this study was p-type (100) Ge with a resistivity of 0.35 Ωcm, corresponding to a substrate impurity concentration of 1×10¹⁶ cm⁻³. Figures 1(a) and 1(b) show the fabrication process of n/p junctions for a source/drain (S/D) on the Ge substrate, and the details are given in Ref. 3.

The gate stack was fabricated using the BLP and subsequent SiO₂-gate insulator fabrication. The details are also given in Ref. 3. The postdeposition annealing (PDA) was carried out at 550°C for 30 min in N₂. Note that the physical thickness of GeO₂ was approximately 2 nm after the PDA.2) A 50-nm-thick TiN was deposited by rf sputtering using a TiN target in Ar ambient. Then, TiN gate electrode area was determined by the patterned photoresist and subsequent wet etching, as shown in Fig. 1(c), followed by PMA at 450°C for 20 min in N₂.4)

As a final processing shown in Fig. 1(d), contacts holes were opened on the S/D region, and Al/Ti electrodes were formed on S/D contacts and gate electrodes by the lift-off process. Then, contact annealing was carried out at 350°C for 10 min in N₂. The reason for the use of TiN contact is to form the low contact resistance to n⁺ S/D regions.3) The EOT (equivalent oxide thickness) of a MOS capacitor in the fabricated n-devices was 42 nm.

3. Result and Discussion

The current-voltage (I-V) characteristic of the fabricated n/p junction is shown Fig. 2, which indicates that a high On/Off ratio of 1.1×10⁸ and an ideality factor of n = 1.1 were achieved. However, the leakage current of the junction with TiN contact is somewhat higher than that with Al.3) This is maybe due to damage during TiN deposition, because the deposition was performed using stronger power of 100 W.

Figure 3 shows the drain current (Iₘ) vs drain voltage (Vₘ) characteristics, where the threshold voltage (Vₜ) was 0.34 V. The result suggests successful operation of TiN-gate n-MOSFET.
the low \( N_d \) region, which is consistent with the results in Ref. 4.

4. Conclusion

TiN-gate n-MOSFET was fabricated on (100) Ge substrate using the gate last process. The MOSFET showed high On/Off ratio of over \( 10^5 \), and the peak electron mobility was \( 1120 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \). This fact comes from effective termination of defects at the SiO\(_2\)/GeO\(_2\) interface and/or in the GeO\(_2\) IL.

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References