Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp891-892

E-2-1(Invited)

In depth characterization of electrical effects of dopants (Al, La, Mg, N) in high-k/metal gate stacks

G. Reimbold[1], M. Cassé[1], X. Garros[1], C. Leroux[1], M. Charbonnier[1], L. Brunet[2,1], S. Baudot[2,1], P. Caubet[2], C. Fenouillet-Béranger[1,2], F. Andrieu[1], O. Weber[1], P. Perreau[1,2], F. Martin[1]

[1] CEA-Leti, Minatec Campus, 17 rue des Martyrs, 38054 Grenoble, France
Phone : +33-4-38784111 Email : gilles.reimbold@cea.fr
[2] STMicroelectronics, 850 rue J. Monnet, 38926 Crolles, France

1. Introduction

Introducing additive (La, Mg, Al) in the gate stack is a well accepted solution to obtain low Vt on transistors of 32 nm node CMOS technologies and beyond [1-2-3]. Controversial results have been published relatively to electrostatic effects as well as quality, reliability and performance of such layers. Using data from a wide panel of experiments (Fig.1 and Fig.2) and focusing on the analysis of the interfacial quality and reliability, this paper will precise benefits and trade-offs obtained through these dopants.

2. Main results

Nitrogen (N). Shifts of threshold voltages are believed to be due to interfacial dipoles or charges at the high-k (HK) / interfacial layer (IL) interface induced by diffusion of dopants throughout the stacks [4-5]. These diffusions towards the SiON/Si interface are believed to create defects affecting the performance and reliability of the transistors. As N may be inserted in all the key stack sub-layers, for example TiN, HfSiON, SiON, it is of crucial importance to quantify its impact. In particular, the impact on drain current can be evidenced by investigating the NBTI and the inversion mobility (Fig.3). Both pMOS NBTI shift and nMOS mobility values are correlated [6] and depend on N concentration and distribution within the interfacial layer. The presence of N at the interface is also correlated to a higher density of interface defects (Nit), with a specific energy distribution. A characteristic peak appears close to the conduction band (Ec), which magnitude is proportional to the amount of diffused N (Fig.4).

Lanthanum & Magnesium for nMOS. The introduction of La could also create extra Nit when La reaches the Si interface. These Nit also show a specific electrical signature with a hump near mid gap (Fig.5), very similar to the well known Pb-centers signature [7]. These additional defects further degrade the mobility. On the contrary, optimized La content does not show any Dit increase while a significant Vfb shift (~0.5 V) and no (weak) mobility degradation can be obtained (Fig.6) [8]. In this case, PBTI is also not degraded compared to La free stacks of good quality (Fig.7).

Mg presents electrical properties close to La, with the ability to shift Vt towards N+ gate [3]. As for La, the effects of Mg on performance and reliability may be studied through the characterization of the Si/oxide interface. For Mg a very specific Dit signature is observed, with a strong hump near Ev and a medium one near Ec (Fig.8).

Aluminum for pMOS. Al doping can induce significant WF_{eff} shifts towards P+: over 0.5V shift is for >3nm SiO_2 layer covered with Al_2O_3 (Fig.9). However in all cases a Roll-off effect strongly reduces the gain due to Al at lower EOT(~1nm) [9]. Thinnest EOT are obtained by introducing Al from metal electrode but WF_{eff} P+ shift due to dipole is modulated due to reduced WF of Al-doped metal (Fig.10).

Comparing TaAlN stacks of Fig.2 we observe a high typical N signature in the gap (Fig.11), enhanced with Al close to SiO_2, while no extra hump due to Al is observed. The cause of this enhanced N signature (confirmed by NBTI Fig.12) remains to understand. Depending on process conditions, Al containing stacks may present broad variations of degradation level (Fig.12). However optimized conditions (thin TiN, low [Al],…) can lead to significant Vt modulation, good reliability (Fig.13), low interface states density and good mobility. Notice than hole mobility is shown to be less affected than electron mobility, especially for short gate length [10]. Moreover Fig.14 shows for TaAlN that for small gate length the discrepancies observed for long channel vanish (edge defects are more critical than Al induced defects). Good mobility values as high as 100 cm^2/Vs may be obtained down to Lg=30nm. Finally defects generated by Al are also shown to be low enough to allow excellent Vt mismatch (A_{VT}<1.5mV.µm) Fig.15.

3. Conclusions

Low Vt control can be efficiently achieved by dopants insertion in the gate stack. However dopants amount and diffusion must be carefully controlled to avoid detrimental effects on drive currents and reliability. In depth analysis of Si/SiON interface can help for a good process optimization.

Acknowledgements

This work has been carried out in the frame of LETI/STMicroelectronics joint Program.

References

[1] V. Narayanan et al., VLSI 2006, p. 178; [2] H.N. Alshareef et al., APL 2006, 072108; [3] K. Ikeda et al., SSDM 2009, p.779; [4] K. Iwamoto et al, VLSI 2007 p.70; [5] J. Robertson and Lin, SSDM 2010 p.667; [6] X. Garros et al, VLSI 2008, p.68; [7].G.J. Gerardi, APL, 1986, p.348; [8] S. Baudot et al., Microelec.Eng. 2010; [9] M. Charbonnier, TED 2010 p. 1809; [10] O. Weber et al, IEDM 2010 p.58.

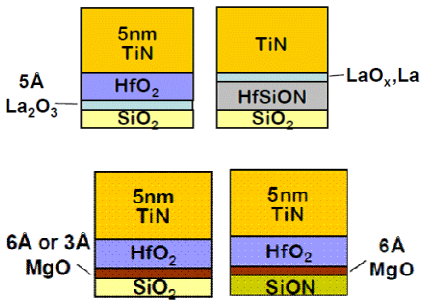

Fig.1 : Main nMOS (La-doped or Mg-doped) stacks discussed in the paper. All devices are annealed at 1050°C.

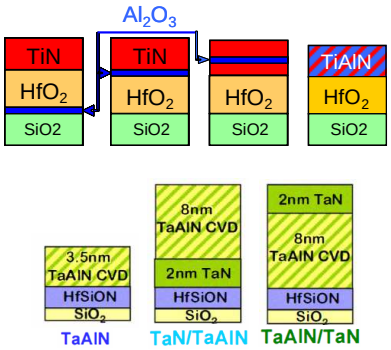

Fig.2 : Main pMOS (Al-doped, Ti or Ta metal) stacks discussed in the paper. All devices are annealed at 1050°C.

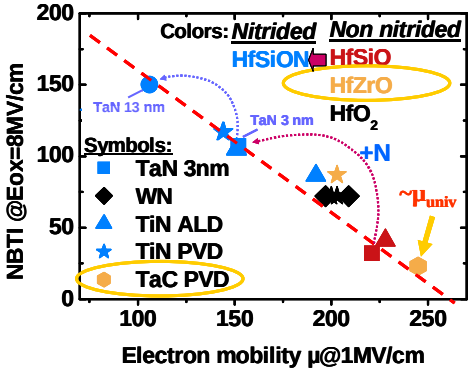

Fig.3: Correlation between PMOS NBTI and nMOS mobility for various gate stack compositions; μ (cm^2/Vs) measured at E=1MV/cm.

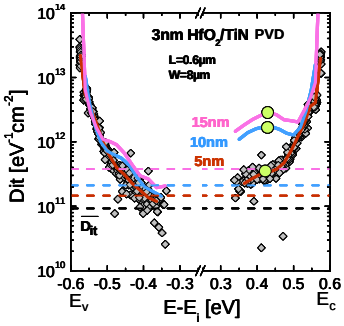

Fig.4: Effect of TiN thickness (5, 10, 15nm) on interface states profiles in the gap. N signature is a hump close to Ec.

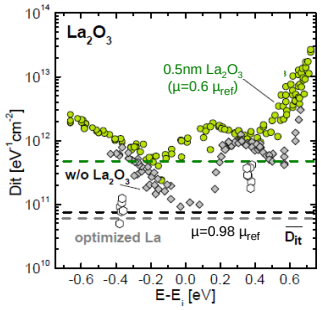

Fig.5: Dit(E) profiles in the gap with no_La /high_[La]/optimized_ La.. Dash lines are mean values in the gap.

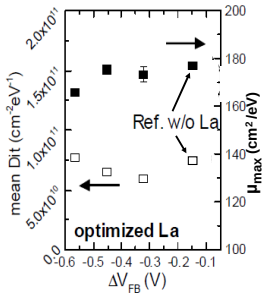

Fig.6: (■) Electron mobility and (□) Dit versus Vfb for various optimized La. Ref. without La is also given.

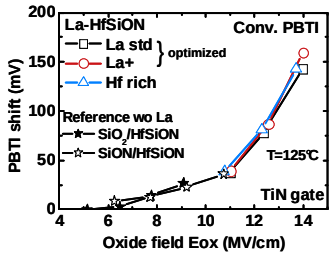

Fig.7: PBTI shift vs. Eox for various optimized [La]. Neither PBTI dependence with La nor extra degradations are seen.

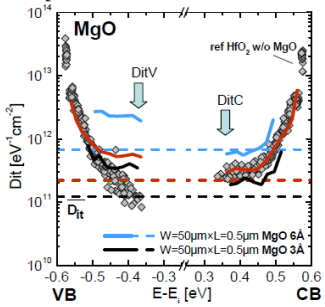

Fig.8: Dit profiles in the gap for various MgO thicknesses. MgO induces a states hump near the silicon valence band.

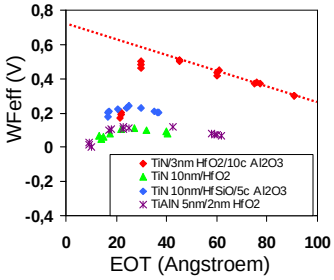

Fig.9: WF_{eff} versus EOT for various Al doping methods in the gate stack. WF_{eff} referred to Si mid-gap. SiO2 interface.

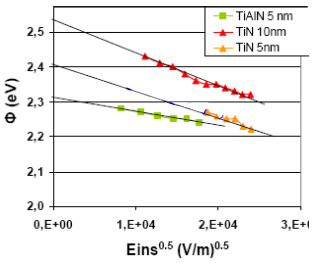

Fig.10: IPE Schottky plot at the metal gate side versus high-k electric field. TiAlN shows smaller barrier (more N+ behaviour) than TiN.

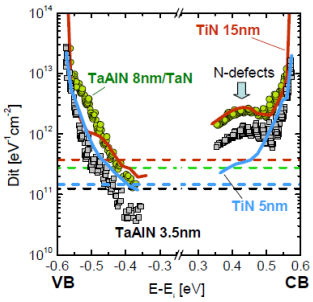

Fig.11: Dit profile in the gap with various stacks w/wo Al. No specific Al signature is observed while N signature is enhanced.

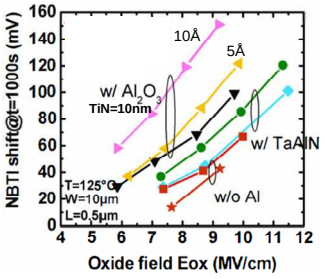

Fig.12: NBTI for various Al incorporation modes and compared to TiN references; stacks of Fig.2. SiO2 interface.

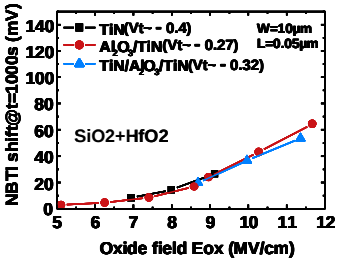

Fig.13 : NBTI(Eox).
Splits on SiO2+HfO2:
■ TiN 10nm ALD
● Al2O3 5Å/ TiN 3nm
▲ TiN 3nm/Al2O3 5Å/TiN 5nm

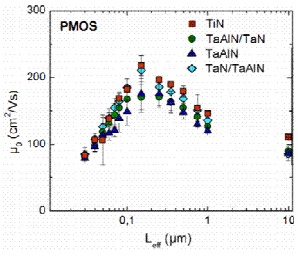

Fig.14 Low field hole mobility versus pMOS gate length (FDSOI). Good μ is obtained for short channels.

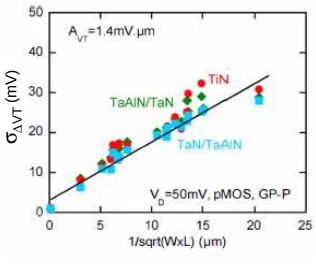

Fig.15 Vt mismatch for TaAlN gates compared to reference TiN / SOI (no doping).