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Impurity Profile Extraction of Semiconductor Devices from STM Tunneling Currents by Current Continuity Based Simulation

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1. Introduction

Current continuity based 3D simulation is applied to impurity profile extraction of semiconductor devices from STM tunneling currents for the first time. A tunnel current between a probe tip and a device is solved consistently with current continuity consideration. Tunneling currents are compared to a pre-made current-concentration table to estimate the concentration at each position. It is revealed that the tunnel current is spread around depletion region which affects the results drastically. A new extraction method ensuring tunneling current values is proposed where the current continuity based STM simulation is iteratively used to get accurate impurity profile even in depletion region.

2. STM Carrier Profiling and Simulation

Carrier profiling is one of the major issue in developing nano-devices. Profiling of device cross sections by scanning tunneling microscopy (STM) has been studied already [1][2][3]. Fig.1 shows an example of STM measurement across a p-n junction. Carrier distribution is deduced from change in STM IV-curves depending on the measured points. Previously, the measurements were modeled by potential-based simulation [4]. Recently we have developed current continuity based 3D modeling as a method to account for the current flow in semiconductor substrate which is critical in quantitative analysis of the STM measurement

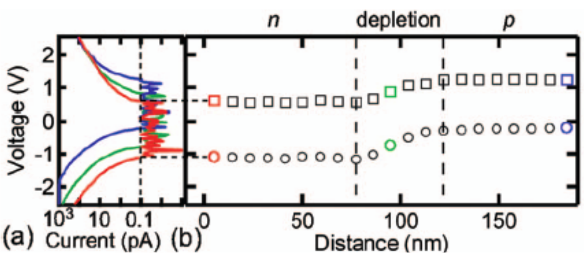

Fig.1 Measured STM I-V curves across a p-n junction [3]. 3 curves in (a) are for same colored positions in(b).

[5].

TCAD system HyENEXSS [6] is used for 3D simulation as shown in fig.2. Carrier tunneling from and into semiconductor conduction and valence bands is included. Not only tip induced band bending is considered [7] but also current flow continuity is automatically included, leading to correct extraction of the impurity profiles from experimental data.

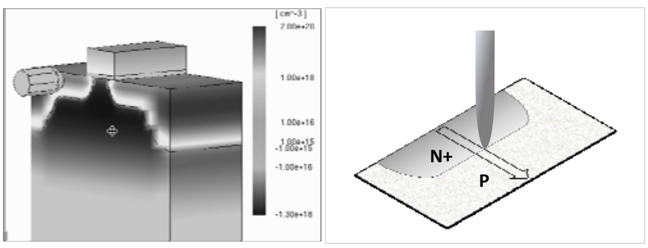

Fig.2 A 3D structure of an STM probe tip and a semiconductor sample created by HyENEXSS (left). Illustration of carrier profiling across a PN junction (right).

STM measurements along a line across an N+ (10^{20}[1/cm^3]) / P (10^{18}[1/cm^3]) abrupt junction are simulated as shown in fig.3, where x<0 is N+ and x > 0 is P-. The tip-sample distance is automatically adjusted by maintaining constant tunneling current at a specified set-point voltage. In this paper, we use set-point voltage Vs=+1.5V and set-point current Is=0.1nA.To know the impurity profile at each point, IV-curves of constant concentration wafers are previously measured as references.

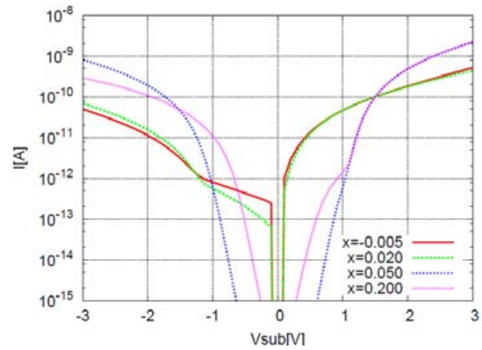

Fig.3 STM IV curves at each position x of the abrupt N+(10^{20})/P(10^{18}) junction. The junction is at x=0

Impurity concentration at each measured points is extracted by comparing target current *It* which is defined as tunneling current at Vsub=-1.0[V]. Fig.4 shows an example of extracted impurity profile for N+(1e20) P-(1e18) abrupt

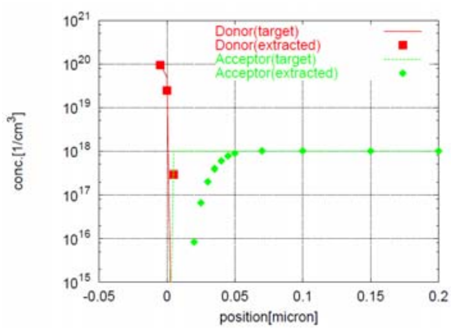

Fig.4 An example of extracted impurity profile of abrupt junction using tip radius of 10nm

junction (sample A). The profiles are consistent with the target distribution excepting the depletion region. As expected, the tunneling current deviates in the depletion region at positions of 0-0.04um owing to 3-dimensional nature of the carriers flow. This problem is tackled by a new iterative extraction method in the next section.

3. Extension and Halo profile

To demonstrate the applicability of the present method, source-drain extension and halo-implanted profiles (sample B) were investigate. The target and extracted profiles are shown in fig.5. In this case, the target current was defined at Vsub=-1.5[V], and the probe tip radius of curvature was 30nm corresponding to a well-prepared tip used in the STM measurements. The extracted profile is reasonably agreed with original profile.

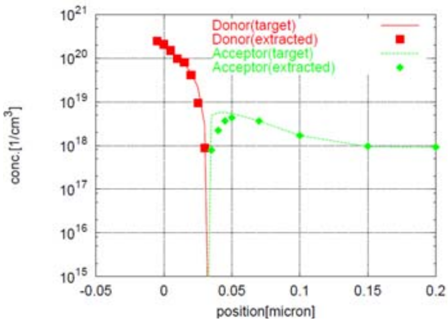

Fig.5 An example of extracted impurity profile of extension and halo profile using tip radius of 30nm

In the depletion region, it is hard to determine the profile because of tip potential and current spreading effects. Fig.6 illustrates inhomogeneous electron density beneath the tip in the depletion region causing diffusion current. This in homogeneity can be adopted in the present current continuity based simulation.

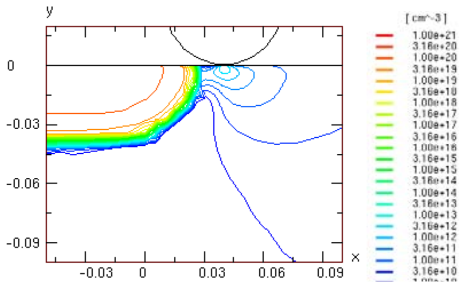

Fig.6 Electron distribution around the probe tip over the depletion region.

To account for the 3D carrier distribution, we correlate the measurement and the simulation. Fig.7 depicts the profile extraction method, where we start with an initial guess, and the impurity concentration at each point is adjusted to eliminate the difference of measured and simulated target currents. It includes not only potential variations but also tunneling current spreading in the depletion region.

Fig. 8 shows results of the impurity profile extraction for sample B. The method results in good matching between the original and extracted impurity profiles across the sample and even in the depletion region. Thus our model and the present procedure successfully explain the physics of the measurement.

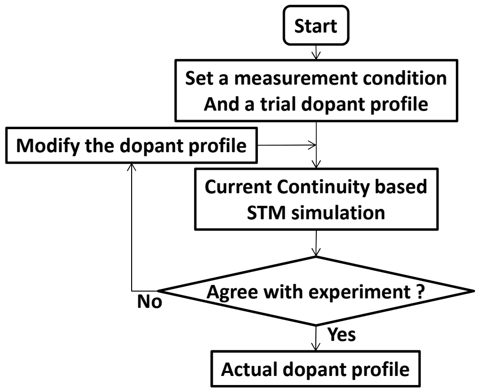

Fig.7 A flow chart of the proposed profile extraction method using current continuity based simulation.

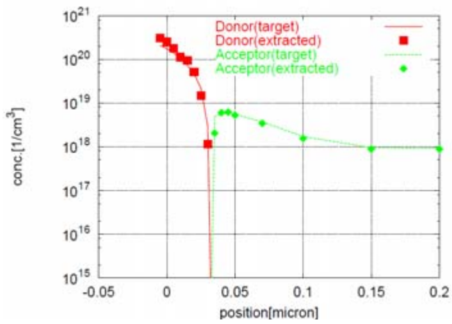

Fig.8 The extracted profile of the same device of fig.5, using presented method. The impurity profile in depletion region is modified sufficiently agreed with the original profile.

4. Conclusions

Current continuity based 3D modeling of STM carrier profiling of semiconductor devices is adapted to extract impurity profiles. STM IV-curves are used to extract the impurity concentration profiles for the two different devices. The developed extraction method gives better matching between the original and extracted impurity profiles even in the depletion region. The results emphasis the necessity of the tunneling current adjustment, and the importance of the iterative procedure for extraction *true* impurity profiles from STM measurements on semiconductor devices.

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