# Influence of channel area scaling on Weibull distribution of TDDB for poly-Si channel FET

Izumi Hirano, Masumi Saito, Toshinori Numata and Yuichiro Mitani

Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation,

8, Shinsugita-Cho, Isogo-ku, Yokohama 235-8522, Japan

Tel/Fax:+81-45-776-5950/4106, E-mail:izumi3.hirano@toshiba.co.jp

### Introduction

Three-dimensional (3D) integration technology has attracted much attention since it gives rise to the higher packing density, shorter interconnection, lower power consumption and heterogeneous device integration[1]. Recently, 3D-FPGA using TFT configuration SRAM over bulk CMOS logic was proposed[2]. Furthermore, it has been reported that the mobility and ON/OFF current of TFT are dramatically improved when the channel area reduces comparable to the grain size[3]. Therefore, the scaled poly-Si channel transistor in combination with high-performance CMOS device is a promising technology to overcome the conventional CMOS scaling limitation. However, long-term reliability, especially the statistical distribution of reliability, of poly-Si channel FET with small area has not been clarified yet.

In this paper, by focusing on the statistical distribution of TDDB for the gate oxide grown on poly-Si with large and small channel area comparing to that on the conventional Si(100) surface, we discuss the guideline in the reliability of gate oxide on poly-Si channel.

#### **Device** fabrication

The devices used in this study were n-channel poly-Si(100) SOI MOSFETs and Si(100) channel SOI MOSFETs. Poly-Si channel were fabricated using following process: 30nm-thick amorphous-Si were deposited after 100nm SiO<sub>2</sub> formation on Si-sub. After that, crystallization by annealing was carried out. Fig.1 shows the plane TEM image of poly-Si channel and histogram of grain size. The grain size of poly-Si was found to be around 130nm. The gate oxides were grown by wet oxidation ambient. Fig.2 shows the variability of gate oxide thickness on Si(100) channel FET and poly-Si channel FET. The average of gate oxide thickness on Si(100) channel FET and poly-Si channel FET were around 3.5nm and 4.5nm, respectively, estimated by CV measurement. The variability of gate oxide thickness for each FETs is less than 2%, indicating that the oxide thickness variability has negligible effect on the TDDB distribution.

## Experimental results and discussion

Firstly we compare the TDDB distribution of poly-Si channel FET to that of Si(100) channel with large channel area, over  $\sim 10^{-8}$  [cm<sup>2</sup>]. These areas were larger than poly-Si grain size. Fig.3 shows the Weibull distribution of Charge to breakdown (Qbd) for poly-Si channel and Si(100) channel for large channel area under positive bias stress. Small  $\beta$  (~1.2) and large  $\beta$  (~1.8) were observed in poly-Si and Si(100) channel, respectively. Fig.4 shows the oxide thickness dependence of Weibull  $\beta$  for poly-Si channel FETs and Si(100) channel FETs. Weibull  $\beta$  strongly depends on tox and the data ( $\beta$ ) reported by several research groups including our experimental data [4,5] follow the same trend in the case of gate oxide grown on Si(100). However, it should be noted that Weibull  $\beta$  for the gate oxide on poly-Si channel is clearly smaller than that on Si(100). These results indicate that the characteristics of defect generation in gate oxide on poly-Si channel is different from Si(100) channel. In order to investigate the behavior of defect generation, we measure the SILC(Stress Induced Leakage <u>Current</u>). Figs.5 (A) and (B) show SILC( $\Delta J/J_o$ ) as a function of injected charge (Qini) for poly-Si and Si(100) FETs with large channel area under various stress voltage. SILC for both FETs shows power law dependence of Qinj and increases with increasing stress voltage. SILC corresponds to defect generation in gate oxide and can be described as SILC =  $\xi (Q_{inj})^{\alpha}$ , where  $\xi$  shows defect creation rate[6,7]. Fig.6 shows the Vg dependence of the defect generation rate,  $\xi$ , for poly-Si and Si(100) FETs. The experimental data for Si(100) reported in the literature [7,8] was also plotted.  $\xi$  of poly-Si FET is larger than that of Si(100) FET, though  $\alpha$  for poly-Si and Si(100) are almost the same value ( $\alpha$ ~0.6), as shown in Figs 6 and 7. From these results, defect in

SiO<sub>2</sub> on poly-Si channel is created easier than that on Si(100) channel, though defects generation process in gate oxide on poly-Si channel are similar to that on Si(100) channel. Therefore, the fragile structure due to poly-Si, i.e., Si surface orientation or grain boundary, dominates the breakdown of SiO<sub>2</sub> on poly-Si channel.

Then we discuss the influence of channel scaling on device characteristics and reliability. Fig.8 shows the channel area dependence of drain current ratio of poly-Si channel to Si(100) channel with various L/W. In larger channel area than 10<sup>-8</sup>cm<sup>2</sup>, I<sub>d</sub> of poly-Si channel FET is smaller than that of Si(100) channel FET. This ratio increases with decreasing channel area especially smaller than 10<sup>-9</sup> cm<sup>2</sup>, indicating that scaling of channel area can mitigate the mobility degradation by grains in poly-Si channel. Then, we investigate the TDDB characteristics of poly-Si channel FET with small area comparable to poly-Si grain size. Fig.9 shows the Weibull distribution of normalized Q<sub>bd</sub> of poly-Si channel for various channel area. Weibull distribution becomes steep, due to decreasing tail of distribution with scaling the channel area. Fig.10 shows the channel area dependence of Weibull  $\beta$  for poly-Si channel FET and Si(100) channel FET. Weibull  $\beta$  were obtained by fitting of all  $Q_{bd}$  data for each device area. In poly-Si channel FET, Weibull ß becomes larger with decreasing of channel area. In addition, Weibull  $\beta$  for poly-Si channel FET with large area is nearly equal to that for Si(110) or Si(111). Weibull  $\beta$  for poly-Si channel FET with small channel area shows almost intermediate value among that on Si(100), Si(110) and Si(111) channel FET.

Fig.11 shows the schematic diagrams of breakdown of poly-Si channel with large channel area and small channel area. In large channel area, as shown in left upper figure of Fig.11, oxide grown on grains of Si(111), Si(110) surface orientation or grain boundary can dominate the extrinsic breakdown in poly-Si FET because these oxides have relatively fragile structures [4]. Therefore, poly-Si channel FET shows wide distribution ( $\beta$ ~1.2). On the other hand, steep distribution  $(\beta \sim 2.4)$  was observed in the larger  $Q_{bd}$  region, shown in right upper figure of Fig.11, corresponding to breakdown of SiO<sub>2</sub> on Si(100). In the case of small FETs, channel area of a FET becomes almost the same with grain size of poly-Si. Therefore, some FETs are probably formed on the single crystalline grains and breakdown characteristics depend on each Si surface orientation. As a result, intrinsic breakdown characteristics of SiO<sub>2</sub> on Si(100) appears in Q<sub>bd</sub> distribution with scaling channel area.

#### Conclusions

In this paper, the influence of poly-Si channel on gate oxide breakdown characteristics was investigated. As a result, in the case of larger channel area comparing to grain size, the Weibull  $\beta$  of poly-Si channel are smaller than that of Si(100) channel This  $\beta$  is almost equal to that on Si(110) or Si(111), indicating that the breakdown of most fragile structure dominate the breakdown in large area poly-Si FET. In addition, the Weibull  $\beta$  of poly-Si become larger with channel area reduced comparable to grain size because intrinsic breakdown characteristics of SiO<sub>2</sub> on Si(100) appears. Further device size scaling, grain size control and orientation engineering of poly-Si can improve the reliability of poly-Si channel devices.

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Fig.6 Defect generation rate ( $\xi$ ) for poly Si channel and Si(100) channel FET with large channel area.  $\xi$  of poly-Si FET is larger than that of i(100) FET.

Fig.7 Power component ( $\alpha$ )of SILC as a function of  $Q_{inj}$  for poly Si channel and Si(100) channel FET with large channel area  $\alpha$  for poly-Si and Si(100) are almost the same value ( $\alpha$ ~0.6).





Fig.9 Weibull distribution of normalized  $Q_{bd}$  of poly-Si channel for various channel area. Weibull distribution of small channel area is steeper than that of large channel area.



Fig.10 Channel area dependence of Weibull  $\beta$  for poly-Si channel FET. The dotted lines show the Weibull  $\beta$  for 4.5nm SiO<sub>2</sub> on Si(100), Si(111) and Si(110) channel[4,5]. Weibull  $\beta$  becomes larger with decreasing of channel area.



Fig.11 Schematic diagrams of breakdown characteristics of poly-Si channel with large channel area and small channel area. In large FET, fragile structure dominates the breakdown of poly-Si FET. In small FET, breakdown characteristics of SiO<sub>2</sub> on single surface orientation of poly-Si appear in Q<sub>bd</sub> distribution.