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On the Si Surface Flattening Effect and Gate Insulator Breakdown Characteristic of Radical Reaction Based Insulator Formation Technology

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1. Introduction

Advantageous characteristics of the radical reaction based insulator formation technology using the microwave excited high density plasma equipment have been reported as follows. 1. Low leakage current density for the direct tunneling regime, about two decades lower than the thermal oxides[1]. 2. Low S-factor variation for FinFET[2]. 3. Higher surface roughness limited carrier mobility and lower 1/f noise than thermal oxides due to the smoother interface[3-6]. 4. Low probability of anomalous stress induced leakage current for tunnel oxinitride lower than thermal oxides[7]. These characteristics lead to the low leakage current interfacial layer formation for high-k gate insulator, gate insulator formation for FinFET logic and low noise analog devices, and high quality tunnel oxides for flash memories with low failure bit probability. However up to now, this technology has not been applied as the gate insulator formation process in the actual LSI manufacturing. The main stumbling block is the higher early failure probability of the radical oxides compared to the thermal oxides when applied to the current manufacturing line. Recently, this was overcome by the introduction of the atomically flat Si surface earlier to the gate oxide formation[8]. Yet, the mechanism of this improvement has not been fully clarified.

In this study, we carefully evaluate the relationships between the Si surface flattening effect and the gate insulator breakdown characteristic of the radical oxidation and the thermal oxidation processes using Si surfaces having various flatness levels before oxidation. This abstract reports on the clarified comprehensive understanding based on the experimental and theoretical analyses, and the important guideline for applying the radical reaction based insulator formation technology to the LSI manufacturing in order to utilize the above mentioned benefits.

2. Experimental Procedure

Fig.1 shows the experimental flow for the evaluations of the surface flattening effect and the gate insulator breakdown characteristics of the radical oxidation and the wet thermal oxidation processes. Cz and epitaxially grown (Epi) n-type Si wafers were used to also evaluate the impact of crystal originated particles (COP) to the breakdown characteristics. The AFM images were taken before the oxidation and after the removal of oxides by HCl/HF mixture solution. This etchant does not etch the surface Si atoms, thus the interface flatness is maintained during the removal of oxides[9]. E_{bd} and Q_{bd} of the fabricated MOS capacitors with the area of 2x2 mm^2 were evaluated.

3. Results and Discussions

Figs.2-3 show the AFM images and the extracted roughness parameter, Ra of the Si surface before oxidation (initial Ra) and of the formed Si/SiO_2 interface (interface Ra). For the radical oxidation, the interface Ra decreases from the initial Ra, and the atomically flatness is maintained. For the wet oxidation, the interface Ra slightly decreases for the initial Ra larger than or equal to 0.12 nm, and increases for the initial Ra smaller than or equal to 0.06 nm. The differences between the initial and the interface Ra are smaller for the wet oxidation than the radical oxidation for initial Ra larger than or equal to 0.12 nm. The schematic illustration of this result is summarized in Fig.4. Here, the initial surface flatness is equivalent to the flatness of top surface of the formed oxides. The atomically flat interface formed by the radical oxidation observed by the transmission electron microscopy (TEM) shown in Fig.5 also validates this result. The strong surface flattening effect of the radical oxidation is also confirmed by the conformal rounding capability of corner regions as shown in Fig.6[10], which is beneficial for the low thermal budget and low Si consumption sacrificial flattening and corner rounding processes.

Fig.7 shows the criterion of the gate insulator breakdown for E_{bd} and Q_{bd} measurements. Figs.8-9 show the E_{bd} as a function of the initial Ra, and the distribution of Q_{bd}. In E_{bd}, the highest values are always higher for the radical oxides than the wet oxides. However, the variation and the minimum values are worse for the radical oxides than the wet oxides for initial Ra larger than 0.12 nm. For the wet oxidation, the initial flatness does not significantly affect the breakdown characteristics. The variation of breakdown in radical oxides is more prominently appeared in Q_{bd} characteristic as the early failure for initial Ra of larger than 0.12 nm. For the initial Ra smaller than 0.06 nm, the intrinsic Q_{bd} of the radical oxides are increased as the initial flatness improves, and the early failure probability is significantly improved especially with the atomically flat surface. Moreover, no significant difference between Cz and epitaxially grown wafers is observed. The roughness due to COP may degrade the breakdown characteristic. However the COP is not the root cause of the early failure of radical oxides. The obtained breakdown characteristics are explained by the simulation results shown in Figs.10-11. For the radical oxides, the excess electric field is significantly increased at the initially concave shaped spots due to the strong interface smoothing effect, which results in the early failures. The obtained results strongly suggest that for the radical reaction based insulator formation technology, the Si surface before gate insulator formation must be sufficiently flattened in order to avoid the early failures.

4. Conclusion

The strong surface flattening effect of the radical oxidation technology is beneficial for the low thermal budget and low Si consumption sacrificial oxidation and corner rounding. However, to apply this technology to the gate insulator formation, the surface before gate oxidation must be flattened so as to avoid the early failure originated from its flattening effect. With this guideline, the advantageous characteristics of the radical reaction based insulator formation technology can be realized in the manufactured LSI.

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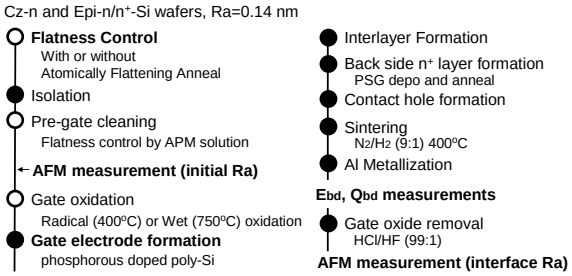

Fig.1 Experimental flow for the evaluations of Si surface flattening effect and gate insulator breakdown characteristics for the radical oxidation and the wet oxidation processes.

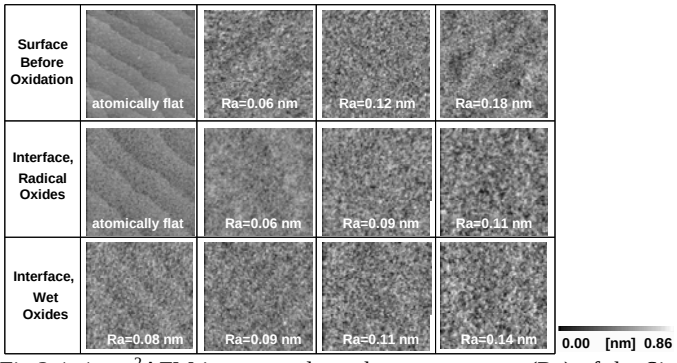

Fig.2 1x1 μm^{2}AFM images and roughness parameter (Ra) of the Si surface before oxidation and Si/SiO_2 interface after removing oxides.

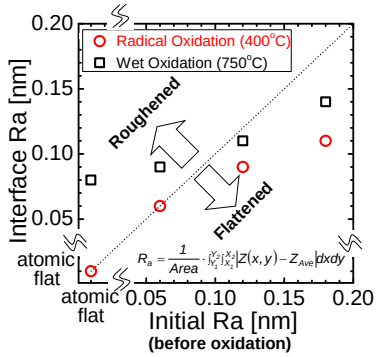

Fig.3 Ra of Si surface before oxidation (initial Ra) and Si/SiO_2 interface (interface Ra).

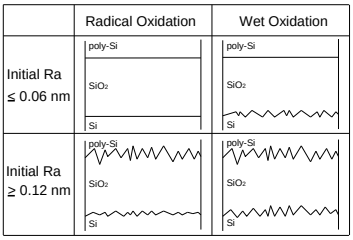

Fig.4 Schematic illustration of cross section of the poly-Si/SiO_2/Si formed by radical and wet oxidations on Si surfaces with different flatness levels.

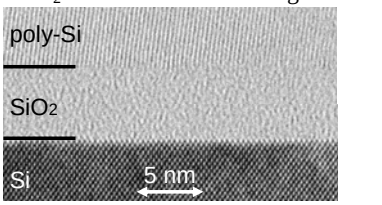

Fig.5 Transmission electron microscopy (TEM) image of poly-Si/SiO_2/Si. The oxide was formed by the radical oxidation on the atomically flat surface. The atomically flat interface is clearly observed.

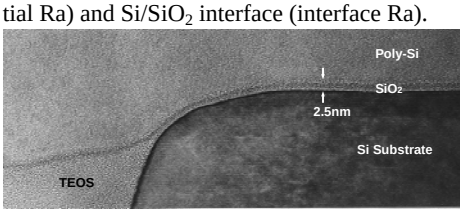

Fig.6 TEM image of thin oxide on the corner of Si formed by the radical oxidation process. The conformal rounding of the corner is obtained.

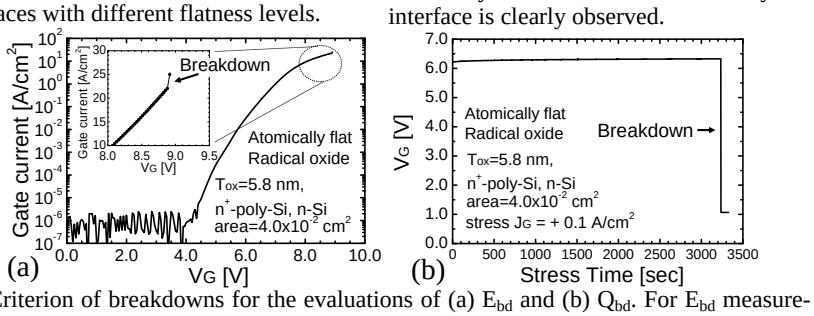

Fig.7 Criterion of breakdowns for the evaluations of (a) E_{bd} and (b) Q_{bd}. For E_{bd} measurement, Epi-wafer with low resistivity substrate and Kelvin probing right above the MOS capacitor electrode were employed to suppress the voltage drop due to the series resistance.

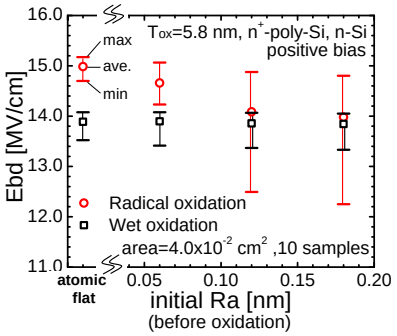

Fig.8 Measured E_{bd} characteristics. A large impact of Si surface roughness before oxidation is clearly observed for the radical oxidation.

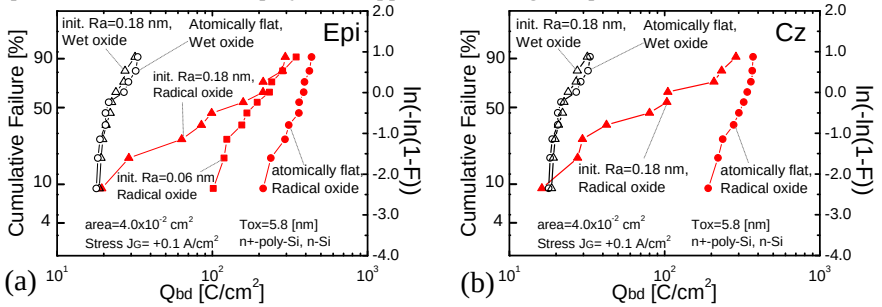

Fig.9 Measured Q_{bd} characteristics on (a) Epi and (b) Cz wafers. The early failure probability is significantly reduced by the introduction of atomically flat Si surface before oxidation. No prominent difference is observed for two wafer types.

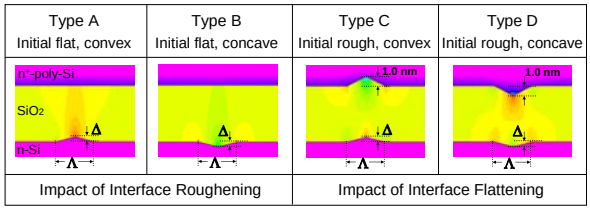

Fig.10 Four types of the simulated poly-Si/SiO_2/Si structures for the evaluation of excess electric field concentration due to the surface roughness before oxidation and due to the interface roughening (type A and B) and the interface flattening (type C and D).

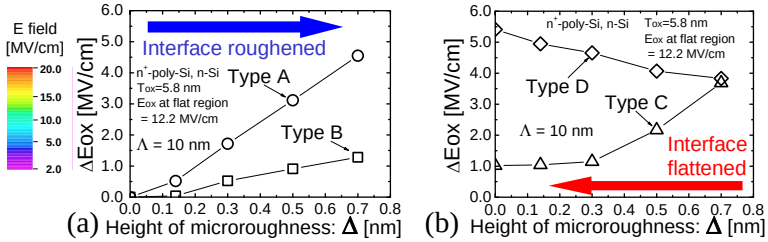

Fig.11 Simulated excess electric field concentration for (a) type A ,B and (b) type C,D. ΔE_{ox} is the highest E_{ox} in each structure subtracted by the E_{ox} at flat regions. For the radical oxidation, a high ΔE_{ox} arises on the initially concave-shaped spots (Type D) which results in the early failures in Q_{bd}.