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High Quality and Low Thermal Budget Silicon Nitride Deposition Using PECVD for Gate Spacer, Silicide Block and Contact Etch Stopper

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1. Introduction

In order to suppress the gate leakage current of MOSFETs and improve the controllability of channel potential, High-k/metal gate has been introduced [1]. In order to reduce the series resistance of source/drain (S/D) electrodes (Rs), new silicide materials have been proposed [2, 3]. New materials used in these processes are in general thermally and chemically unstable. Thin insulator films to protect the introduced material from various chemical solutions during integration process are required in order to avoid the chemical instability of the introduced materials. And these protection films must be deposited at a low temperature to avoid the thermal instability. SiN is widely used for various steps of LSI fabrication such as the gate spacer, silicide block layer and contact etch stop layer to integrate these new materials [4]. For this purpose, a high selectivity against SiO_2 during dry and wet etching and a sufficient step coverage are strongly required for SiN film deposited at low temperature below 400ºC. It has been reported that the atomic layer deposition (ALD) and plasma enhanced chemical vapor deposition (PECVD) can deposit SiN at low temperature [5]. Although SiN deposited by ALD is high quality at low deposition temperature, the deposition rate is low, which limits the productivity. Although SiN deposited by conventional PECVD is high quality on blank Si wafer due to the effect of ion bombardment, SiN at the sidewall of stepped shape is poor and local void arises due to low step coverage as shown in Fig. 1. In this work, we improve the quality of SiN at the sidewall of stepped shape deposited by PECVD at 400ºC up to a compatible level to ALD while keeping the higher deposition rate by supplying a large amount of the species for nitridation and the avoiding the ion bombardment damage against SiN which can be realized by PECVD using a microwave excited high density and low electron temperature plasma [6]. The developed high quality SiN deposition process is applied to the fabrication of CMOS with the dual silicide using W/$ErSi_2$ and W/Pd_2Si, and the obtained characteristics are reported.

2. Experimental procedure

SiN was deposited on both blank Si surface and patterned poly-Si surface at 400ºC by PECVD using the micro-wave excited high density plasma [6]. Before SiN deposition, Si wafers were cleaned by 0.5% diluted HF to remove the native oxide on Si surface, rinsed in ultra pure water (UPW) and chemical oxide was formed on Si surface in ozonated UPW. The thickness and refractive index of the deposited SiN were measured by a spectroscopic ellipsometer operating from 248 to 827 nm. 0.5% HF etch rate of the deposited SiN on the blank Si surface and the sidewall of patterned poly-Si were evaluated by the spectroscopic ellipsometer and scanning electron microscopy (SEM), respectively. Fig. 2 shows the process flow of the CMOS circuits with dual silicide. After S/D junction was formed, 10 nm-radical oxidation at 400ºC and 50 nm-SiN deposition were carried out to form the sidewall spacer. After the silicide was formed for p-MOSFET, 50 nm-SiN was deposited to protect p-MOSFET silicide (W/Pd_2Si) from wet solutions such as sulfuric acid-hydrogen peroxide mixture (SPM) and diluted HF (DHF) during the n-MOSFET silicidation. After silicide was formed for n-MOSFET, 50 nm-SiN was deposited as the contact etch stop layer. All of the SiN deposition was performed at 400ºC in order to avoid the thermal instability of the silicides.

3. Results and Discussions

Fig. 3-5 show the deposition rate and the refractive index at 633 nm wavelength as functions of the deposition pressure, SiH_4 and H_2 flow rate, respectively. The refractive index become almost ideal value of 2.03, as the quality of SiN improves. The deposition rate and refractive index increase as the process pressure increases as shown in Fig. 3. It is considered that Si and N precursors are more produced at a lower pressure because electron temperature relatively increases as the deposition pressure decreases. The deposition rate is proportional to the SiH_4 flow rate as shown in Fig. 4, and it indicates that the deposition rate in this process is limited by SiH_4 supply. However the refractive index increases as SiH_4 flow rate decreases. It is considered that the quality of SiN in this process is limited by the supply of N precursor against Si precursor, and it increases due to the increase of gas flow ratio of N_2/SiH_4. The refractive index decreases as H_2 flow rate decreases less than 15 sccm and increases as H_2 flow rate increases over 30 sccm in Fig. 5. It was found that the appropriate range of H_2 flow rate exists and it is 15 to 30 sccm in this process. 0.5 % HF etch rate is shown in Fig. 6. The HF etch rate is lower, as quality of SiN improve by the decrease of SiH_4 flow rate The low HF etch rate of 0.4 nm/min and the deposition rate of 1.3 nm/min at SiH_4 flow rate of 0.5 sccm were obtained. The properties of SiN deposited by various equipments are summarized in table 1 [4, 8, 9]. SiN deposited in this work shows low HF etch rate compatible to those of ALD and even LPCVD. Fig. 7 shows (a) the schematic and (b) the SEM images of MOSFETs after etching of SiN to form the sidewall. Fig. 7 (c) and (d) show the SEM images of MOSFETs after the samples were dipped in ozonated UPW and HF solution to evaluate HF etch property of the sidewall SiN. The deposited SiN conditions were SiH_4 flow rate of (c) 3.0 and (d) 0.5 sccm. In the case of SiH_4 flow rate of 0.5 sccm, the shape of SiN sidewall is remained almost the same before and after HF solution and the 25-nm sidewall is stably formed. Fig. 8 shows the SEM images of the fabricated CMOS during the integration process. After etch stop SiN is deposited on W/$ErSi_2$ is formed for n-MOSFET silicide, these samples were dipped in HF solution. The SiN is deposited with SiH_4 flow rate of (a) 3.0 sccm and (b) 0.5 sccm. In the case of 0.5 sccm, $ErSi_2$ is not etched by HF and the HF resistance of SiN is shown to be sufficiently high to be used as the protection film for $ErSi_2$. The CMOS ring oscillator with dual silicide S/D was fabricated using the developed 400ºC SiN deposition process as the gate spacer, silicide block and contact etch stopper. Fig. 9 shows the speed performance of the ring oscillator as a function of applied voltage. The short delay time is obtained due to ultra-low Rs by the introduction of dual silicide and high current drivability of Si(551) accumulation-mode device structure [3].

4. Conclusions

We improve the quality of SiN by supplying a large amount of N precursor using PECVD using the micro-wave excited high density plasma equipment. To increase N precursor against Si precursor, the deposition pressure and SiH_4 flow rate decrease and H_2 flow rate were optimized. Low HF etch rate of 0.4 nm/min is successfully achieved with a SiN deposition rate of 1.3 nm/min. The developed high quality SiN deposition process was applied to the gate spacer, silicide block and contact etch stop layer formations for CMOS with an advanced dual silicide, and its effectiveness is confirmed by the high speed performance of the fabricated ring oscillator.

References

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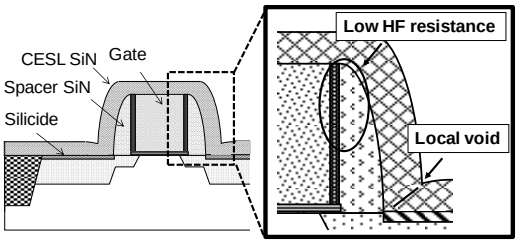

Fig. 1. Issues of conventional PECVD for CMOS fabrication. Quality of SiN at sidewall is poor and local void arises due to low step coverage.

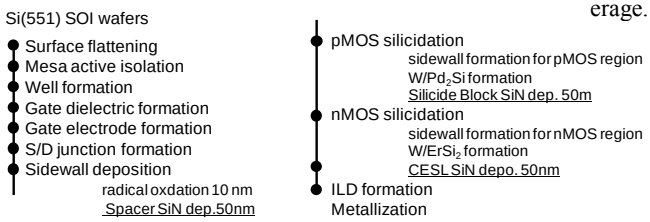

Fig. 2. Process flow of the CMOS with the dual silicide S/D. SiN deposition was performed three times for sidewall formation, pMOS silicide protection layer from wet solution and for contact etch stop layer. All of the SiN deposition was carried out at 400ºC.

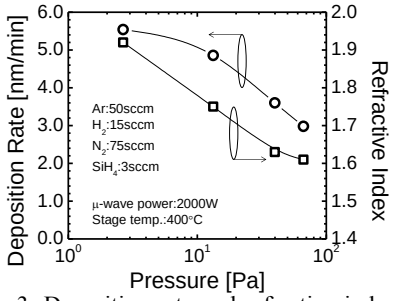

Fig. 3. Deposition rate and refractive index as a function of deposition pressure. The deposition rate and refractive index increase as the process pressure increases.

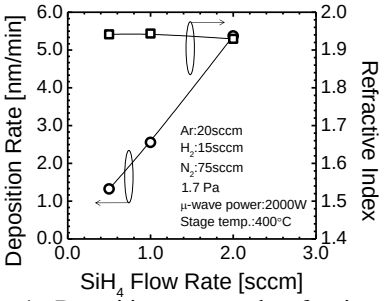

Fig. 4. Deposition rate and refractive index as a function of SiH_4 flow rate. The deposition rate is limited by SiH_4 flow rate. The refractive index increases as SiH_4 flow rate decreases.

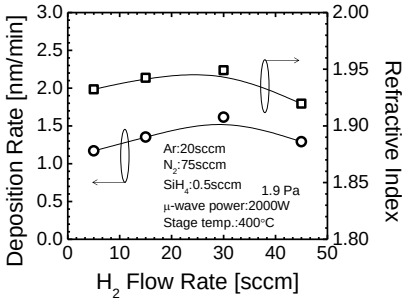

Fig. 5. Deposition rate and refractive index as a function of H_2 flow rate. The refractive index decreases as H_2 flow rate decreases less than 15 sccm and increases as H_2 flow rate increases over 30 sccm.

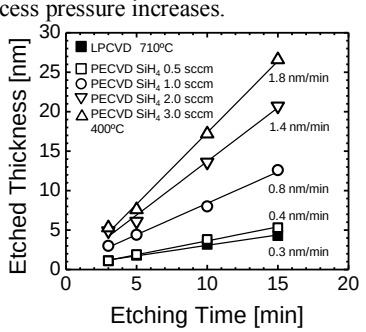

Fig. 6. Etched thickness of SiN as a function of the 0.5 % HF etching time. The evaluated samples were deposited at SiH_4 flow rate of 0.5, 1.0, 2.0 and 3.0 sccm. The HF resistance improves as SiH_4 flow rate decreases.

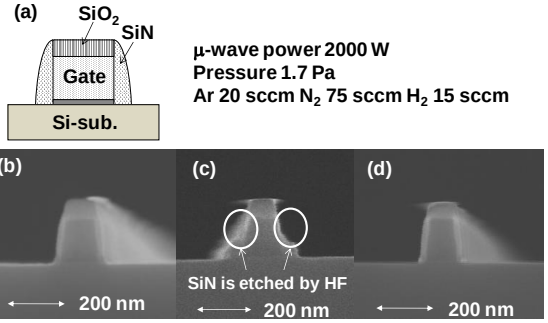

Fig. 7. (a) Schematic and (b) the SEM images of MOSFETs after forming SiN sidewall by dry etching, and (c), (d) followed by wet treatment 0.5 % HF for 1 min, ozonated UPW for 5 min and 0.5 % HF for 3min to evaluate the HF resistance of SiN sidewall. SiN was deposited at SiH_4 flow rate of 3.0 and 0.5 sccm in (c) and (d).

Table 1. Dep. temp. and 0.5 % HF etch rate of SiN deposited by various equipments. HF etch rate is calculated at 0.5 % HF as shown in [10].

	temp.[ºC]	etch rate [nm/min]	ref.
LPCVD	710	0.3	—
ALD 1	375	2.4	[8]
ALD 2	550	0.8	[9]
ALD 3	595	0.6	[4]
PECVD (This work)	400	0.4	—

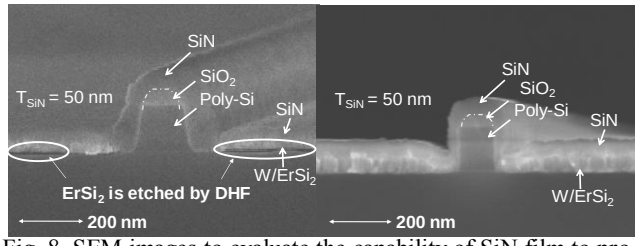

Fig. 8. SEM images to evaluate the capability of SiN film to protect W/$ErSi_2$ from chemical solution. Samples were dipped in 0.5 % HF for 3 min. SiN were deposited at (a) 3.0 sccm and (b) 0.5 sccm of SiH_4 flow rate. $ErSi_2$ is easily etched by HF with the etch rate of several μm/min. In (a), HF solution penetrated from the pattern edge and etched $ErSi_2$. In (b), no etching of $ErSi_2$ is confirmed.

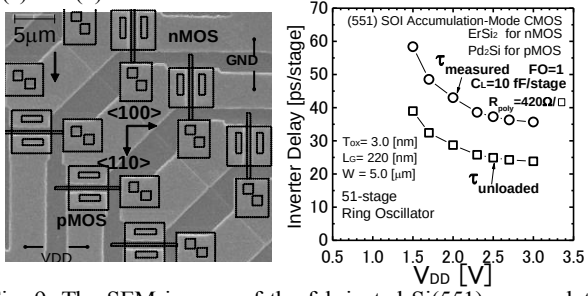

Fig. 9. The SEM images of the fabricated Si(551) accumulation CMOS ring oscillator with dual silicide (a), and measured stage delay time as a function of the applied voltage. High speed performance is obtained due to the reduction of Rs and the enhancement of carrier mobility.