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Strained Ge Layers on SiGe(Sn) Buffer Layers Formed by Solid-phase Mixing Method

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1. Introduction

Biaxial compressive strained Ge (st-Ge) can be expected to improve on the hole mobility in channel of metal-oxide-semiconductor field effect transistors (MOSFETs). The fabrication of the $Si_{1-x}Ge_x$ on insulator (SGOI) is one of key technologies for st-Ge MOSFET. Some fabrication methods for SGOI have been reported [1, 2]. We previously reported that the formation of strain-relaxed SGOI structure with solid-phase mixing the heteroepitaxial Ge layer and Si on insulator (SOI) over 1000°C [3]. Recently, we also found that Sn incorporation in a Ge layer is effective to reduce in the annealing temperature to as low as 400°C for solid-phase mixing [4]. However, the mechanism of solid-phase mixing phenomena in the $Ge_{1-z}Sn_z$/SOI structure has not been understood in detail. Also, we have to clarify the crystalline properties of st-Ge layers grown on these SGOI substrates.

In this study, we investigated the influence of the Sn content and SiO_2 cap layer thickness on the solid-phase mixing between $Ge_{1-z}Sn_z$ and SOI. We also examined the growth of a st-Ge layer on SGOI substrates and investigated its crystalline properties.

2. Experiment

The substrates used were low-doped separation by implanted oxygen (SIMOX) wafers with a SOI thickness of 40~44 nm. After chemical and thermal cleaning of a substrate, a $Ge_{1-x}Sn_x$ layer with a thickness of 59~320 nm was epitaxially grown on the SOI substrate at a substrate temperature of 150~200°C with molecular beam epitaxy (MBE) method. The Sn content of $Ge_{1-x}Sn_x$ layers was ranging from 0 to 10.8%. A SiO_2 capping layer with a thickness of 14~140 nm was deposited on samples, and then samples were annealed at 300~1000°C for 1~180 min in N_2 ambient.

In addition, we prepared st-Ge/SGOI samples with a $Si_{1-x}Ge_x$ thickness of 154 or 190 nm and Ge content of 0.7 or 0.5 (samples A~C as shown in Table I). After removing the SiO_2 cap layer and thermal cleaning of the surface, a 20 nm-thick st-Ge layer was epitaxially grown on SGOI at a substrate temperature of 200°C~300°C.

3. Results of discussion

Inter mixing between $Ge_{1-z}Sn_z$ and SOI layers

Figure 1 shows the out-of-plane lattice constant of the epitaxial layers as a function of the annealing time for $Ge_{1-z}Sn_z$/SOI samples. The annealing temperature for $Ge_{0.892}Sn_{0.108}$/SOI and $Ge_{0.933}Sn_{0.67}$/SOI was 400°C and for $Ge_{0.97}Sn_{0.03}$/SOI was 500°C. For samples with a higher Sn content, the lattice constant more rapidly decreases smaller than that of bulk Ge at lower temperature, indicating that solid-phase mixing between $Ge_{1-z}Sn_z$ and SOI and the formation of $Si_{1-x-y}Ge_xSn_y$ layers preferentially occur.

Figure 2 shows predicted and measurement values of the substitutional-Sn content in $Si_{1-x-y}Ge_xSn_y$ layers. The measurement values were estimated from x-ray diffraction two-dimensional reciprocal space map (XRD-2DRSM) measurement. The measured substitutional-Sn content is much lower than the predicted values assuming all Sn atoms are at the substitutional sites in $Si_{1-x-y}Ge_xSn_y$. Figures 3(a)-3(b) show scanning electron microscope (SEM) images of those samples after etching the SiO_2 cap layer with HF solution. We can observe etch pits as dark areas. They are considered to be the evidence after etcing precipitated Sn grains. Hence, Sn atoms precipitate after the solid-phase mixing of $Ge_{1-z}Sn_z$ and SOI because of the solid-solubility of Sn as low as about 1% in Si and Ge.

Figure 4 shows the lattice constant of the epitaxial layers as a function of the annealing time for samples with a SiO_2 cap layer whose thicknesses are 14 and 140 nm. The solid-phase mixing more rapidly occurs for the sample with a thicker SiO_2 layer. We suggest that a compressive stress in the $Ge_{1-z}Sn_z$ layer from the SiO_2 cap layer due to the difference of their thermal expansion coefficients enhances the solid-phase mixing.

Strained Ge layers grown on SGOI substrates

Figure 5 shows the XRD-2SRSMs results for the st-Ge/$Si_{0.3}Ge_{0.7}$ on insulator (sample A). The SGOI was prepared with annealing Ge/SOI at 900°C ~1000°C. Table I is the summary of crystalline properties evaluated from XRD-2DRSM and atomic forth microscope (AFM) measurements for st-Ge/SGOI samples. The strain value for the sample A was estimated to be 0.47%, while those for samples B and C were as low as 0.2%. The strain value is smaller for the sample with larger ΔTilt of the $Si_{1-x}Ge_x$ layer. Large ΔTilt means large mosaicity with introducing dislocations in the $Si_{1-x}Ge_x$ layer. This result means that the strain relaxation of a Ge

layer is enhanced with the dislocations in the $Si_{1-x}Ge_x$ buffer layer. In addition, in the case of sample C, the strain relaxation preferentially occurs with introducing misfit dislocations due to the larger lattice mismatch between Ge and $Si_{0.5}Ge_{0.5}$ layers than $Si_{0.3}Ge_{0.7}$. On the other hand, the sample B shows large surface RMS roughness of the st-Ge layer. This result suggests that the strain relaxation is additionally caused with the surface roughening of st-Ge layer.

4. Conclusions

We found that the lager Sn content and thicker SiO_2 cap layer effectively enhances the solid-phase mixing between the $Ge_{1-z}Sn_z$ and SOI to form $Si_{1-x-y}Ge_xSn_y$. We also demonstrated that the control of the mosaicity and surface roughening of SGOI is a key to obtain a st-Ge with a large strain value and small mosaicity.

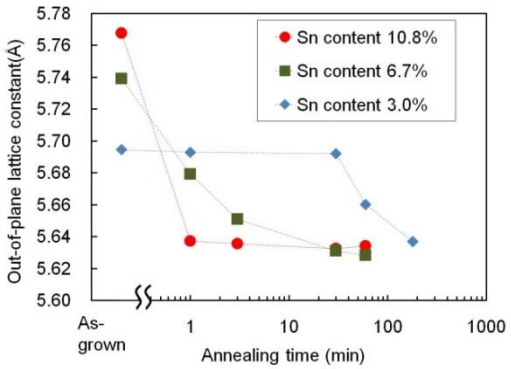

Fig. 1 Out-of-plane lattice constant of the $Si_{1-x-y}Ge_xSn_y$ layer as function of annealing time for $Ge_{0.97}Sn_{0.03}$/SOI, $Ge_{0.933}Sn_{0.67}$/SOI and $Ge_{0.892}Sn_{0.108}$/SOI samples.

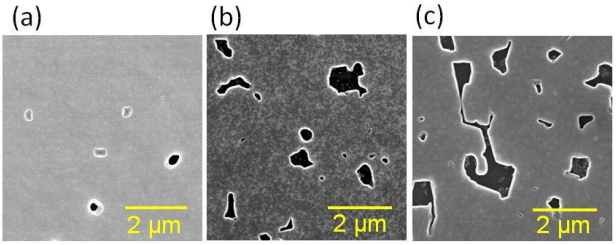

Fig. 3 The planer SEM image of (a) $Ge_{0.97}Sn_{0.03}$/SOI, (b) $Ge_{0.933}Sn_{0.67}$/SOI and (c) $Ge_{0.892}Sn_{0.108}$/SOI samples.

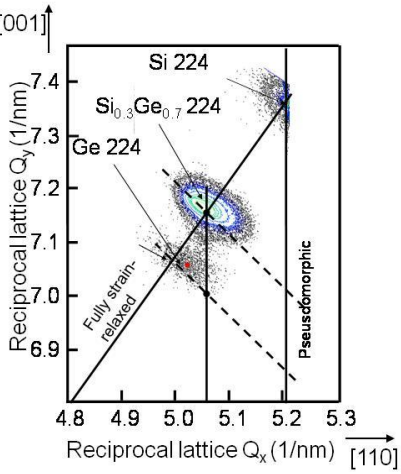

Fig. 5 XRD-2DRSM of the stained $Ge/Si_{0.3}Ge_{0.7}$ on insulator sample (sample A).

Acknowledgement

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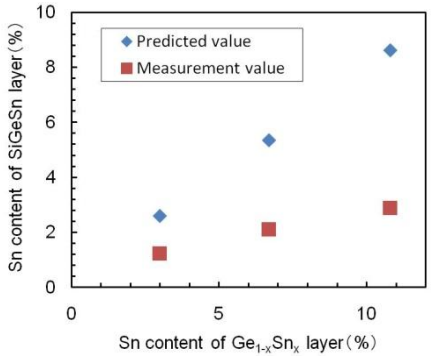

Fig. 2 Predicted and measurement values of Sn contents of $Si_{1-x-y}Ge_xSn_y$ layers after solid-phase mixing.

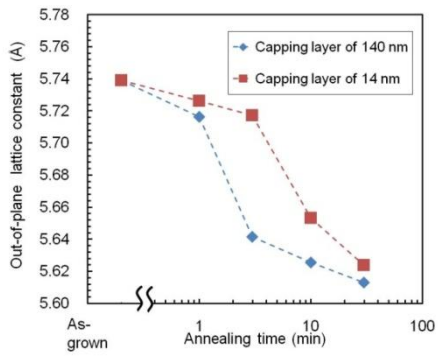

Fig. 4 Out-of-plane lattice constant of the $Si_{1-x-y}Ge_xSn_y$ as function of the annealing time for $SiO_2/Ge_{0.933}Sn_{0.67}$/SOI with a SiO_2 thickness of 14 nm and 140 nm.

Table I Summary of the crystalline structure of $Si_{1-x}Ge_x$ and strained Ge layers for samples A~C.

Sample	A	B	C
Ge composition (%)	70	70	50
$Si_{1-x}Ge_x$ thickness (nm)	154	190	119
Strain of Ge (%)	0.47	0.23	0.26
ΔTilt of $Si_{1-x}Ge_x$ (deg.)	0.23	0.55	0.4
ΔTilt of st-Ge (deg.)	0.89	1.05	1.18
RMS roughness (nm)	1.1	4.1	1.9