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Formation of Ultra-thin and Uniform Ni-InGaAs Alloyed Contact for Scaled Metal S/D InGaAs MOSFETs

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Abstract

Thickness controllability and thermal stability of Ni-InGaAs alloyed contact have been investigated with the aim of the applications to scaled metal S/D InGaAs MOSFETs. Low sheet resistance (~25 Ω/□) Ni-InGaAs alloyed layers with the thickness as thin as 6 nm, which meets the requirement of scaled metal S/D MOSFETs (Lg < ~50 nm), have been formed by reducing evaporated Ni thickness and annealing temperature. It was found that the ultra-thin and smooth alloyed layer maintained after additional annealing at temperatures up to 250˚C. These results suggest that low temperature BEOL processes (< 250˚C) would enable us to utilize Ni-InGaAs alloyed contacts in scaled metal S/D devices.

Introduction

High mobility InGaAs channel nMOSFETs are attractive for high-speed and low-power CMOS applications which cannot be realized by conventional Si technologies [1,2]. One of the critical challenges in InGaAs MOSFETs is a formation of low resistance S/D contacts by a self-aligned manner. Recently, a SALICIDE-like contact technology using Ni-InGaAs alloy has been proposed and metal S/D InGaAs nMOSFETs with very low Schottky barrier height have been demonstrated [3,4]. However, thickness controllability and thermal stability of those alloyed layers have not been well investigated yet. So far, only thick alloyed layers (> 30 nm) have been reported to be formed even after low temperature annealing (250˚C, 1 min) due to high reactivity of Ni with InGaAs, while sufficiently thin layers (< ~10 nm) is desired for scaled metal S/D MOSFETs (L_g < ~50 nm) with suppressed short channel effects.

In this study, we have evaluated thickness controllability of Ni-InGaAs alloyed contacts through a precise control of the amount of evaporated Ni and annealing conditions and low sheet resistance (~25 Ω/□) and uniform Ni-InGaAs alloyed layers with thickness as thin as 6 nm have been successfully obtained. Thermal stability of Ni-InGaAs alloyed layers has also been investigated to evaluate the BEOL process window.

Experimental

Ni with the thickness of 4, 7, and 12 nm was deposited by electron beam evaporation on p-$In_{0.53}Ga_{0.47}As$ (N_a = 2 x 10^{17} cm^{-3}) grown on p-InP substrates. Evaporated Ni thickness (t_{Ni}) was much thinner than that of previous work (30 nm [3]) because targeted layer thickness is less than 10 nm in this work. After evaporation, rapid thermal annealing (RTA) under Ar ambient was performed at 200 - 500˚C for 1 min. Formed Ni-InGaAs alloy was characterized by TEM, EDX and sheet resistance measurements. It was confirmed by TEM and EDX after annealing that there was no unreacted Ni in all samples even without wet etching of Ni. Long-time (10 min) annealing experiments after metallization were also performed to assess the thermal stability of the Ni-InGaAs alloyed layers.

Results and discussion

Fig. 1 shows the annealing temperature (T_a) dependence of Ni-InGaAs alloyed layer thickness ($t_{Ni\text{-}InGaAs}$) as a parameter of initial evaporated Ni thickness (t_{Ni}). Standard deviation (σ) of $t_{Ni\text{-}InGaAs}$ for t_{Ni} = 4 nm is also plotted. It is seen that $t_{Ni\text{-}InGaAs}$ decreases with decreasing T_a and t_{Ni}, and Ni-InGaAs alloyed layers with $t_{Ni\text{-}InGaAs}$ as thin as 6 nm can be formed in cases of t_{Ni} = 4 nm, T_a < 250˚C. Fig. 2 shows TEM pictures of samples for t_{Ni} = 4 nm, T_a = (a) 200˚C, (b) 300˚C, (c) 400˚C. Uniform alloyed layers (σ = 0.6 nm) are confirmed at T_a = 200˚C while interface roughening occurred with increasing T_a ($T_{Ni\text{-}InGaAs}$ in Fig.1 are average values). On the other hand, such rough interface is not seen for T_{Ni} = 12 nm, T_a = 400˚C (Fig. 2 (d)). These results suggest that Ni shortage during RTA induces interface roughening and that low T_a and thin t_{Ni} is essential to obtain thin alloyed layers with smooth interface.

Fig. 3 shows the T_a dependence of sheet resistance ($R_□$) of Ni-InGaAs alloyed layers as a parameter of t_{Ni}. The values of as-deposited samples are also shown for comparison. Here, metallic layers (Ni or Ni-InGaAs) were dominantly measured because of the high Schottky barrier height between metals and p-InGaAs [3]. $R_□$ drastically decreases after RTA and the values as low as 25 Ω/□ are obtained even in the samples with $t_{Ni\text{-}InGaAs}$ = 6 nm (t_{Ni} = 4 nm, T_a < 250˚C). This value is low enough for scaled metal S/D devices and almost the same as that of previous reports [3,4] in spite of the fact that $t_{Ni\text{-}InGaAs}$ in this study is much thinner. From these results, it can be confirmed that thin Ni-InGaAs alloyed layers with low $R_□$, which meets the requirement of scaled metal S/D MOSFETs, are formed through the control of t_{Ni} and T_a. Fig. 4 shows the T_a dependence of resistivity (ρ) of Ni-InGaAs alloyed layer as a parameter of t_{Ni}, deduced from the data of Figs. 1 and 3. It is found that ρ increases with increasing T_a and t_{Ni}. The increase of ρ with increasing T_a is considered to be due to the interface roughening as seen in Fig. 2 and/or the chemical composition change (Ni and Ga decrease while As increases) as detected by EDX (Fig. 5). On the other hand, such chemical composition change due to different t_{Ni} was not observed (data not shown) and the reason for increased ρ with increasing t_{Ni} at fixed T_a has not been clearly understood at present. Different t_{Ni} might cause some structural differences, e.g. phases, crystallinity and grain sizes.

Thermal stability of thin Ni-InGaAs alloyed layers against long-time thermal budget during the BEOL processes has also been investigated. Fig. 6 shows TEM pictures of samples annealed for 10 min at (a) 200˚C, (b) 250˚C, (c) 300˚C, (d) 400˚C. Here, 6-nm Ni-InGaAs alloyed layers were formed prior to 10 min annealing. It is confirmed that thin layer (< 10 nm) with the smooth interface (σ < 1.1 nm) are preserved up to T_a = 250˚C. No distinct chemical composition change was also confirmed at T_a = 250˚C. On the other hand, similar to Fig.2, interface roughening and $t_{Ni\text{-}InGaAs}$ increase take place above T_a = 300˚C. These results suggest that Ni-InGaAs alloyed layers are thermally unstable and low temperature BEOL processes are required for real scaled metal S/D device applications.

Conclusion

Thin Ni-InGaAs alloyed layers (6 nm) with low sheet resistance (25 Ω/□), meeting the requirement of scaled metal S/D devices, were formed thorough the control of the amount of evaporated Ni and annealing conditions. Low temperature BEOL processes (< 250˚C) would be a key to fully exploit the attractive properties of Ni-InGaAs alloyed contacts in the scaled metal S/D devices.

Acknowledgement

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References

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[3] S. H. Kim et al., IEDM Tech. Dig., 26.6 (2010).
[4] X. Zhang et al., ECS Solid-State Lett., **14** (5), H212 (2011).

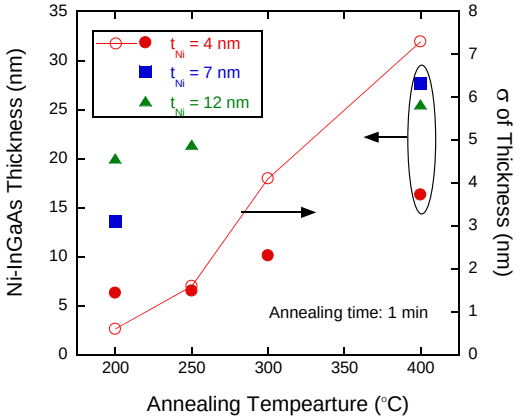


Fig. 1 Annealing temperature (T_a) dependence of Ni-InGaAs alloyed layer thickness as a parameter of initial evaporated Ni thickness (t_{Ni}). Standard deviation of layer thickness for t_{Ni} = 4 nm is also shown.

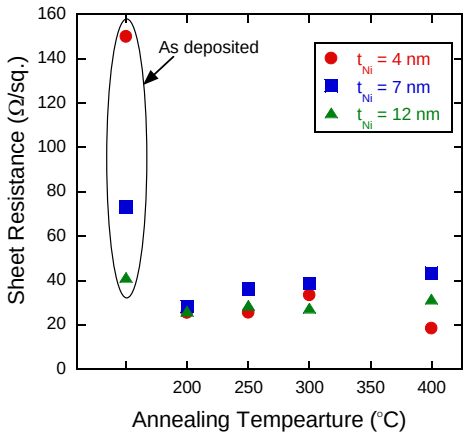
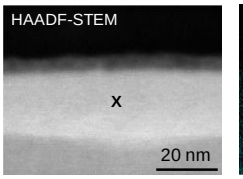
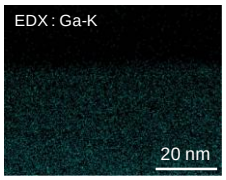


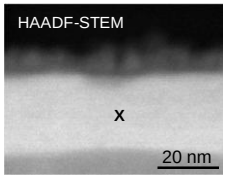
Fig. 3 Annealing temperature (T_a) dependence of sheet resistance of Ni-InGaAs alloyed layer as a parameter of evaporated Ni thickness (t_{Ni}).

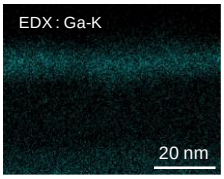




	at. %
Ni	46.6
In	16.5
Ga	9.0
As	18.7

(a) Ni:12 nm, Ta = 200˚C





	at. %
Ni	39.3
In	19.1
Ga	4.0
As	28.8

(b) Ni:12 nm, Ta = 400˚C

Fig. 5 HAADF-STEM and EDX (Ga-K) pictures of samples for t_{Ni} = 20 nm, (a) T_a = 200˚C, (b) 400˚C. Chemical compositions (at %) of Ni-InGaAs alloy measured by EDX are also shown.

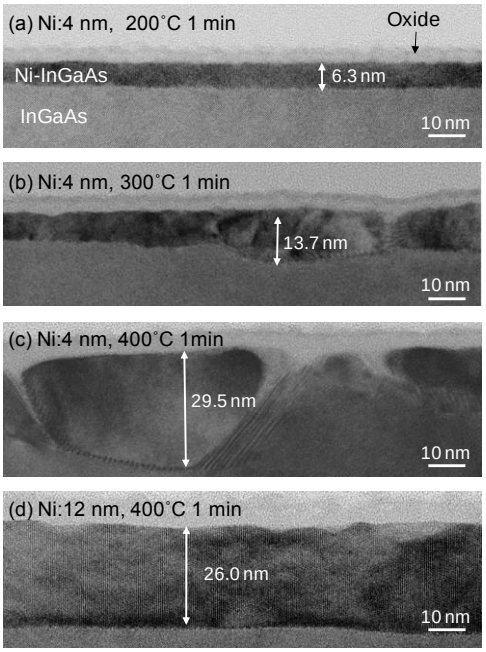


Fig. 2 TEM pictures of samples for T_{Ni} = 4 nm, (a) T_a = 200˚C, (b) 300˚C, (c) 400˚C.

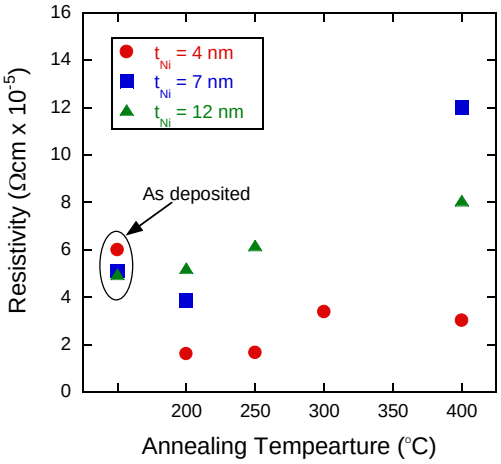


Fig. 4 Annealing temperature (T_a) dependence of resistivity of Ni-InGaAs alloy as a parameter of evaporated Ni thickness (t_{Ni}).

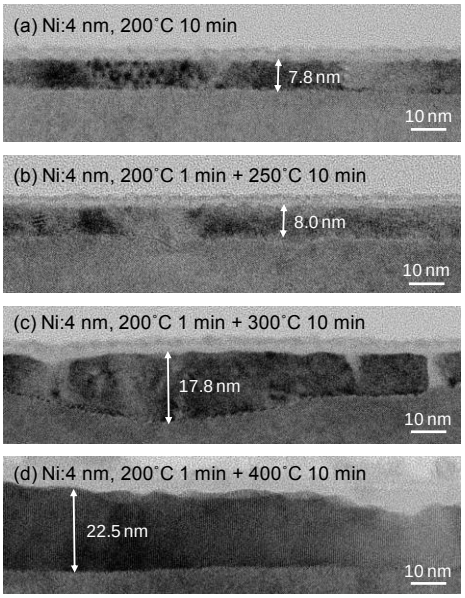


Fig. 6 TEM pictures of samples for t_{Ni} = 4 nm, (a) T_a = 200˚C 10 min, (b) 200˚C 1 min + 250˚C 10 min, (c) 200˚C 1 min + 300˚C 10 min, (d) 200˚C 1 min + 400˚C 10 min..