Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp949-950

Silicon-On-Insulator Fabrication Using Si/HfO_2/Si Epitaxial Structure

Shinji Migita and Hiroyuki Ota

Green Nanoelectronics Center (GNC), National Institute of Advanced Industrial Science and Technology (AIST)
West 7, Onogawa16-1, Tsukuba Ibaraki 305-8569, Japan
E-mail: s-migita@aist.go.jp

1. Introduction

Silicon-on-insulator field-effect transistor (SOI FET) with ultra-thin buried-oxide (BOX) layer is a promising device structure because the back gate bias contributes to the suppression of short-channel effect, the reduction of variation, and the tuning of threshold voltage [1-3]. Ultra-thin BOX is also useful to enhance the tunnel-FET performance by double-gate operation [4]. Although the thinnest BOX layer in commercial SOI has achieved 10 nm recently, a further scaling of BOX thickness is anticipated in these applications.

In this paper, we propose an approach to fabricate ultra-thin BOX using high-k film in place of SiO_2 in SOI structures. Through simulations and examinations, the advantage of high-k BOX is discussed.

2. Concept of Silicon-On-high K (SOK)

Figure 1 shows SOI FET devices integrated using high-k film as the BOX layer. We named this structure "Silicon-On-high K (SOK)." The SOK is fabricated on bulk Si wafers. Starting from the isolation and the back gate formation by ion implantation and anneal, high-k layer and Si layer are prepared by deposition techniques. SOK FETs are fabricated using the top Si layer. Owing to the large dielectric constant of high-k film, the equivalent oxide thickness of BOX (EOT_BOX) can be reduced than its physical thickness.

The impact of BOX thickness scaling for 10 nm-gate length SOI FETs was studied by TCAD simulation (Fig. 3(a)). It is found that 10 nm-gate length SOI FETs require BOX thickness less than 10 nm (Fig. 3(b) and (c)). High-k BOX is thus attractive to achieve sub-10 nm EOT_BOX while suppressing the leakage current. It is noticed that a trade-off exists between the reduction of leakage current and the suppression of DIBL by high-k BOX (Fig. 3(d)).

3. Experimental

The SOK structure was fabricated by sequential deposition of HfO_2 and Si films on Si substrate. N-type Si (111) wafers with 0.1 Ω-cm resistivity were used. Firstly, the surface region of Si wafers was heavily doped by phosphorus ion implantation and activation anneal (10^{19} /cm^3). Following to the removal of oxides on Si surfaces by dilute HF solution, HfO_2 films were deposited by atomic-layer deposition and annealed at 800°C to crystalize epitaxial HfO_2 films on Si [5]. Si films were deposited on HfO_2 surfaces by chemical vapor deposition at 650°C using Si_2H_6 gas.

4. Results and Discussion

Figure 2 shows a cross-sectional TEM image of Si/HfO_2/Si structure. Thickness of each layer is uniform and their interfaces are smooth. A thin SiO_2 layer is formed at the HfO_2/Si interface, which might be caused by the diffusion of oxygen through HfO_2 layer after crystallization. TEM images of respective layers were analyzed by fast Fourier transformation. Symmetric spots demonstrate successive epitaxial growth of HfO_2 film on Si and Si film on HfO_2.

Scalability of the BOX thickness by epitaxial HfO_2 film was investigated by MOS capacitors (Fig. 4(a)). NiSi electrode was formed by patterning the top Si layer and silicidation. Reasonable *C-V* curves were obtained although stretch out and hysteresis must be improved (Fig. 4(b)). Owing to the dielectric constant of HfO_2 film, EOT_BOX could be scaled to less than 10 nm still they include SiO_2 interfacial layers (Fig. 4(c)).

Feasibility of the SOK structure was investigated by back-gate operation of MOS FET (Fig. 5(a)). After isolation of the top Si layer, NiSi was formed at source and drain region. Modulation of drain currents by back gate bias (Fig. 5 (b)) and drain bias (Fig. 5(c)) are observed. Because of the Schottky barrier height of NiSi (4.7 eV), the MOS FET shows p-type operation. Thus the top-Si layer is applicable as a channel of SOI FET.

5. Conclusions

BOX scaling less than 10 nm will be demanded for advanced MOS FETs and new FETs such as tunnel-FETs. The SOK that has a high-k BOX layer is helpful to achieve ultra-thin BOX with low leakage current. The SOK is advantageous because it can be fabricated in-house using conventional deposition tools. It will bring flexibility in design of VLSI chips.

Acknowledgements

The research is granted by the Japan Society for the Promotion of Science (JSPS) through the "Funding Program for World-Leading Innovative R&D on Science and Technology (First Program)," initiated by the Council for Science and Technology Policy (CSTP).

References

[1] T. Hiramoto *et al*., Jpn. J. Appl. Phys. **42** (2003) 1975.
[2] N. Sugii *et al*., Jpn. J. Appl. Phys. **48** (2009) 04C043.
[3] C. Fenouillet-Beranger et al., 2010 Symp. VLSI Tech., p.65.
[4] K. Boucart and A. M. Ionescu, IEEE TED **54** (2007) 1725.
[5] S. Migita *et al.*, IEDM Tech. Dig., 2010 p. 423.

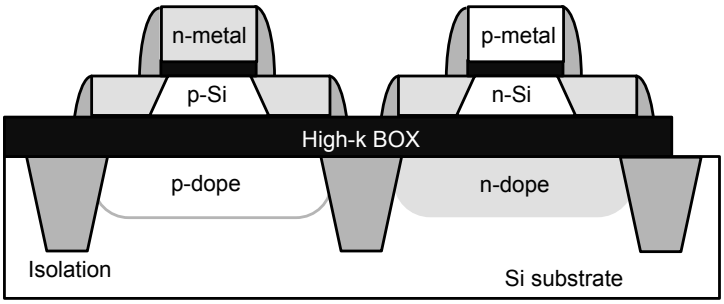

Fig. 1 Proposal of Silicon-On-high-K (SOK) structure for SOI FET fabrication with ultra-thin BOX layer. The high-k BOX layer contributes to the BOX_EOT scaling while suppressing the leakage current.

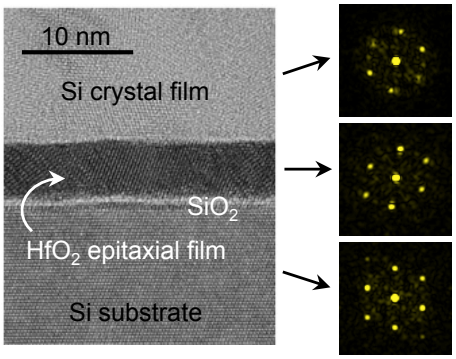

Fig. 2 Cross-sectional TEM image of Si/HfO_2/Si structure and fast Fourier transformation pictures of respective layers.

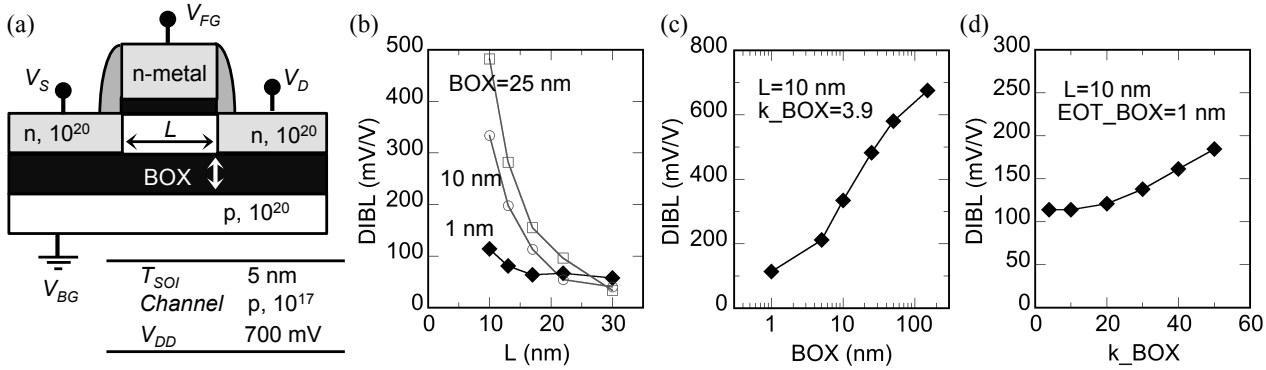

Fig. 3 (a) TCAD simulation of 10 nm-gate length SOI FET with ultra-thin BOX. (b) Drain induced barrier lowering (DIBL) vs. gate length. DIBL becomes serious at gate length less than 20 nm. (c) DIBL vs. BOX thickness. Sub-10 nm BOX thickness is required to suppress DIBL. (d) Impact of the dielectric constant of BOX layer (k_BOX) on DIBL at a fixed EOT_BOX (1 nm). DIBL gradually increases with higher-k.

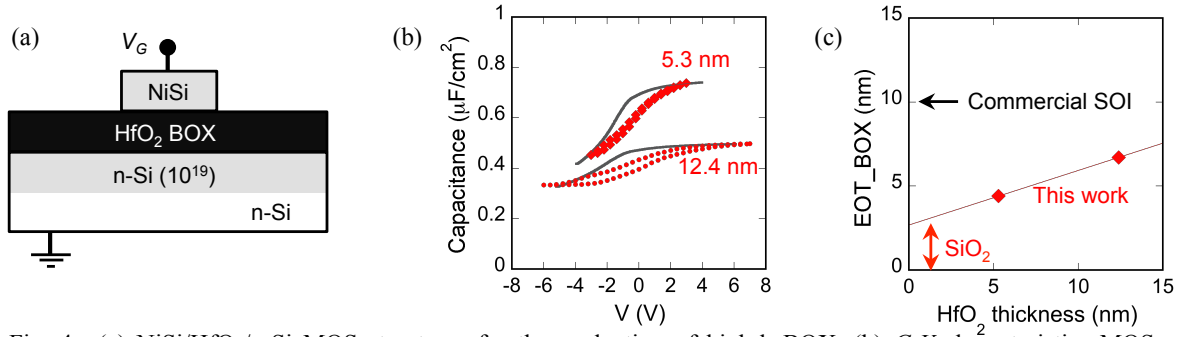

Fig. 4 (a) NiSi/HfO_2/n-Si MOS structures for the evaluation of high-k BOX. (b) *C-V* characteristics MOS capacitors. HfO_2 thicknesses are 5.3 nm and 12.4 nm. Solid lines show simulations. (c) BOX_EOT vs. physical thickness. EOT less than 10 nm is achieved by high-k BOX.

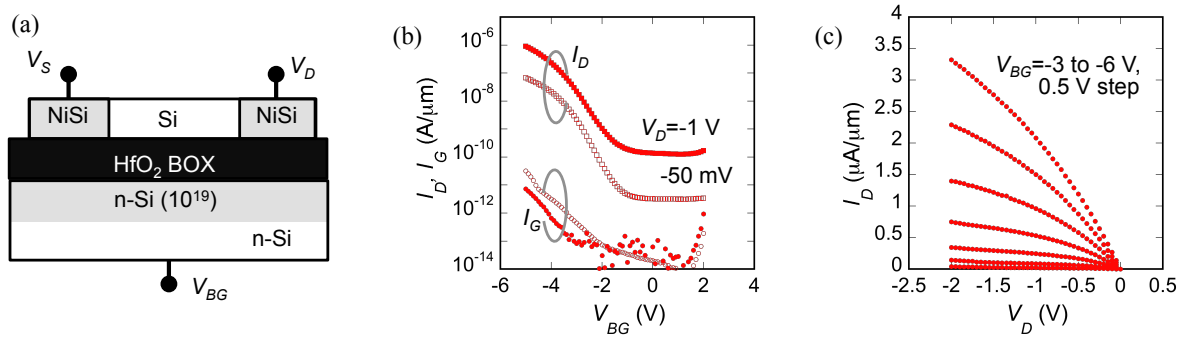

Fig. 5 (a) Fabricated MOS FET using Si/HfO_2/Si structure. Thicknesses of HfO_2 and Si are 12.4 nm and 24 nm, respectively. Heavily doped Si substrate was used as the back gate. NiSi was formed at source and drain region. The gate length is 1 μm. (a) I_D-V_{BG} and I_G-V_{BG} curves. (b) I_D-V_D curves.