# Enabling epitaxy on ultrathin implanted SOI

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## I. INTRODUCTION

In Fully Depleted Silicon On Insulator (FDSOI) transistors, the channel thickness is being scaled down with the gate length to insure a good electrostatic control of the gate over the channel. Typically for the 20nm node, the transistor integrity is maintained by keeping the channel thickness below 6nm [1]. This downscaling raises several technological challenges, especially when using an integration scheme in which extensions are implanted *before* the Raised Source and Drain (RSD) growth (Fig. 1). The challenge lies in finding a viable tradeoff between amorphization and high dopant concentration within the film. In this paper we present what are the main physical limitations when implanting the SOI, as well as an efficient way to alleviate them.

# II. CHALLENGES FOR THIN SOI FILM INTEGRITY AFTER DIRECT IMPLANTATION

Doping the extension before RSD growth is appealing because it allows following standard integration flow and it is expected to induce low dopants dispersion. Indeed, using this approach, not only the ion implantation is done on a well controlled SOI silicon thickness but also the implantation energy is low (1-2keV) and therefore the dopants straggle. However the defects created in the SOI by implantation may strongly impact RSD growth quality, eventually leading to defective growth as shown in Fig.2 with a dramatic decrease of the electrical performance (Fig.3). Even though defective growth can be evidenced by SEM observations, in this paper ellipsometric measurements were preferred as a systematic, fast, and non destructive technique. In particular the goodness of the fit (GOF) was used to quantitatively evaluate film quality, as already proposed [2,3]. Fig.2 shows that wafer locations where RSD morphological quality is excellent have GOF values always exceeding 0.99 whereas wafer locations where RSD morphological quality degrades and epitaxy roughness increases undergo a GOF value decrease below 0.99. To investigate further the origin of the epitaxy quality degradation, the GOF value after RSD epitaxy was plotted as a function of the SOI thickness before epitaxy measured at the exact same location. For each 300mm SOI substrate patterned with 22nm design rules, 49 points were recorded across the wafer. The results are shown in Fig.4 for SOI implanted directly with arsenic (As). On the un-implanted SOI reference wafer, the GOF values after epitaxy are constant and above 0.99 whatever the SOI thickness value before epitaxy. This is consistent with the excellent RSD quality observed in the SOI thickness range down to 3nm. When the SOI layer undergoes direct As implant prior to RSD growth, a clear drop of the RSD GOF value is observed below a critical SOI thickness t<sub>c</sub>. This drop in GOF matches with the onset of RSD quality degradation shown in SEM image of Fig.2. At fixed As implant energy of 1keV, the t<sub>c</sub> value increases from 4nm to 5nm when the dose increases from  $3 \times 10^{14}$  at.cm<sup>-2</sup> to  $1.5 \times 10^{15}$  at.cm<sup>-2</sup>. The morphological degradation of the thin silicon layer is correlated to electrical behavior through sheet resistance R<sub>s</sub> measurements. As shown in Fig.5, R<sub>s</sub> as a function of the SOI thickness departs from the expected  $\rho/t_{SOI}$ 

trend below a t<sub>c</sub> value that is proportional to the implanted dose. Fig.6 shows that both methods (GOF and R<sub>s</sub>) lead to the same t<sub>c</sub> vs dose behavior. The onset of electrical and morphological degradation is clearly correlated to the SOI amorphization thickness estimated by C-TRIM simulations [4]. As a consequence a way to reduce t<sub>c</sub> is to reduce the amount of defects induced by the implantation. For a given implant condition it can be achieved by splitting the dose. Fig.4 shows that by implanting 3 times  $5 \times 10^{14} \text{at.cm}^{-2}$ with intermediate 600°C re-crystallisation annealings rather than by implanting  $1.5 \times 10^{15} \text{ at.cm}^{-2}$  the amorphisation thickness and therefore the t<sub>c</sub> values are consistently reduced. However, even with dose splitting, when using direct implantation t<sub>c</sub> can hardly be decreased below 4nm. For 5-6nm thick channels, taking into Si consumption all over the process, t<sub>c</sub> has to be pushed down to insure a reliable process at the wafer scale.

## III. INTEREST OF IMPLANT THROUGH A SCREEN LAYER

The benefit of implanting through a screen nitride layer is presented in Fig.7. This approach is very attractive not only to leave most of the implant related defects in the screen layer (Fig.7a) but also to tailor the dopants profile in the SOI (Fig.7b). Ultimately, the SOI can even benefit from a higher dose than in the direct implant case, while the dopants level in the BOX will be kept very low. The dopant dose left in the SOI is plotted as a function of the nitride liner thickness in Fig.8 for a 1.5x10<sup>15</sup>at.cm<sup>-</sup> As implanted dose at 1keV. The calculations are done for 3nm and 5nm SOI thickness. For those implant conditions a 2-3nm thick nitride screen layer is a good comprise to reduce the film amorphisation to 1nm or less while keeping a high dose in the SOI. Interestingly, in this screen nitride thickness range, the dose in the SOI does depend neither on SOI thickness nor on liner thickness. Therefore, the use of a liner can accommodate SOI thickness variation as far as the dopant dose incorporated is concerned. Fig.9 shows clear experimental evidence of the interest of using a screen nitride layer to alleviate the limitations of direct implantation on SOI. The same ellipsometric measurement technique as the one proposed in Fig.4 is used. For a significant number of wafers, it is observed that the onset of GOF degradation (t<sub>c</sub>) can be lowered to ~2nm for an As dose ranging from  $3x10^{14}$ at.cm-2 to  $1.5x10^{15}$ at.cm<sup>-2</sup>, whereas with direct implantation  $t_c$  is ~4nm or ~5nm respectively. Similar trends (not reported here) are observed for P or BF<sub>2</sub> implanted SOI.

### IV. CONCLUSION

Using simple ellipsometric measurements, it is evidenced that direct implantation in ultra thin SOI has intrinsic limitations as subsequent RSD growth quality together with  $R_s$  are degraded. It is possible to alleviate very efficiently these limitations by depositing a thin nitride layer prior to implantation, allowing SOI films as thin as 2nm to be doped as high as  $1.5 \times 10^{15}$  at.cm<sup>-2</sup> while still being able to grow high quality monocrystalline RSD on top of these doped SOI films.



➡ SEM top down Ellipsometry SEM cross section very local very local local destructive semi-statistical statistical non destructive non destructive fast GOF mapping after RSD growth 0.98 Good epitaxy

Figure 1: Simplified FDSOI integration flow, in which the extensions are implanted before the RSD growth.



Fig.3: Normalized Ion-Ioff characteristics of two wafers having the same process except for the extension implantation where blue squares corresponds to higher energy leading to partial amorphisation in the extension region.



Fig. 6: (left)  $t_c$  as determined by GOF (solid symbols) and Rs (open symbols) and (right) amorphisation thickness as determined by CTRIM simulations for different Arsenic doses implanted in the SOI at 1keV.



Fig. 8: Dose left in the SOI and related amorphization thickness as a function of the nitride thickness deposited prior to implant (C-TRIM). SOI is either 3nm (blue circles) or 5nm (red squares) thick.

Figure 2: GOF mapping after RSD epitaxy and correlation with SEM inspections at different locations on a 300mm patterned SOI wafer.

10

10

10<sup>3</sup> L 3.5

4.0

(Ω/square)

Rs



Figure 4: RSD GOF as a function of SOI thickness before RSD. Data correspond to SOI implanted with Arsenic at 1keV with different doses from  $3x10^{14}at.cm^{-2}$  to  $1.5x10^{15} at.cm^{-2}$ , in comparison to a non implanted SOI reference.



SOI thickness (nm) Figure 5: Sheet resistance measurements as a function of the SOI thickness. Data correspond to SOI implanted with Arsenic at 1keV with different doses from 3x10<sup>14</sup>at.cm<sup>-2</sup> to 1x10<sup>15</sup>at.cm<sup>-2</sup>. Solid

4.5

As / 1keV / 3e14cm

As / 1keV / 5e14cm As / 1keV / 1e15cm

5.0

5.5

 $\rho_1 / t_{cr}$ 

6.0

ρ,



Figure 7: (a) Defects density and (b) Arsenic concentration calculated from CTRIM (As, 1keV, 1.5.10<sup>15</sup>at.cm<sup>-2</sup>) implanted either directly into the SOI (blue) or through a 3nm nitride screen layer. The SOI thickness is taken to be 3nm. The defects density is decreased of more than one decade without any penalty in terms of dopant loss within the SOI film.



Fig. 9: RSD GOF as a function of SOI thickness before RSD. Data correspond to SOI implanted with different Arsenic doses a 1keV, either through a 3nm nitride liner (open symbols) or without any liner (solid symbols).

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### VI. REFERENCES

- V. Barral et al, IEDM 2007, C. Fenouillet-Beranger et al, SSE, p. 961, 2004.
- [2] L. Clavelier et al., ECS, 2005
- [3] C. Le Royer et al., SOI Conf, 2006
- [4] M. Posselt et al, Mat. Sc. and Engineering B, vol. 71, Issues 1-3, p. 128, 2000