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Performance and Variability Comparisons between ALD- and PVD-TiN Gate FinFET

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Introduction

As one of the promising metal gate materials for FinFETs, titanium nitride (TiN) has been widely studied for realizing symmetrical V_{th} without channel doping [1-3]. Recently, it was reported that a metal induced stress affects the FinFET mobility [4] and a work function variation (WFV) of metal gate is the dominant source of V_{th} variation for the undoped FinFET [5]. However, less studies have been done on the process dependence of TiN deposition on the FinFET performance [6]. In this paper, we have experimentally explored the impact of TiN gate stack process, i.e, atomic layer deposition (ALD) or physical vapor deposition (PVD), on the mobility and V_{th} variation for the FinFETs.

Experiment

Figure 1 shows a process flow of the FinFET fabrication. As a starting material, (100) oriented SOI wafers were used. First, vertical fin channels were formed in parallel with <110> direction by EB-lithography and RIE. After gate oxidation, a TiN was deposited by ALD or PVD methods. For ALD case, a TiN was deposited using the alternate supply of tetrakis dymethylamino titanium (TDMAT) and NH_3 [7]. For PVD case, TiN was deposited by RF magnetron sputtering. After TiN deposition, 85-nm-thick n^+-poly-Si layer was deposited as the gate capping layer. Figure 2 shows cross-sectional TEM view of the fabricated FinFETs with ALD- and PVD-TiN gates. It is clear that TiN thickness on the fin-side channel is thinner for PVD case compared to ALD case due to less conformality of PVD TiN. As a result, a TiN thickness just on the side channel was 25 nm for ALD, while 10 nm for PVD. After the gate formation, ion implantation (I/I) and rapid thermal annealing (RTA) was performed.

Results and discussion

The SEM view of the fabricated FinFET is shown in Fig. 3. It is clealy seen that scaled gate structure wih a length (L_g) of 40 nm is successfully fabricated. Figure 4 shows split–CV characteristics of the multi-FinFETs. From this result, the CETs of ALD- and PVD-TiN gate FinFETs are estimated to be 2.06 and 1.93 nm, respectively. Figure 5 shows an electron mobility of the fabricated FinFETs. It can be seen that an electron mobility for the ALD case is lower than that for PVD case. This degradation is probably due to thicker TiN on the side of fin channel for ALD case. It is already reported that a compressive stress becomes higher with increasing TiN thickness [4]. This stress degrades the performance of <110> nFET with (110) channel surface. Figure 6 shows the measured typical I_d-V_g characteristics of the fabricated FinFETs with the same L_g = 80 nm. It is clear that almost an ideal S-slope is obtained for both ALD- and PVD-TiN gate FinFETs. Also both exhibit an identical short channel effect (SCE) immunity as shown in Fig. 7. The difference of V_{th} between ALD and PVD cases is probably due to the different TiN thickness. Previous literature reported that the V_{th} increases as the TiN thickness increases due to negative charge [8]. Next, the L_g dependence of the mobilty is investigated based on the channel resistance (R_{ch}) – L_g relationship at the same overdrive voltage (V_{od}) of 0.6 V as shown in Fig. 8. The parasitic resistance, which is estimated from the on-resistance (R_{on})-L_g plots, is subtracted from R_{on} to estimate the R_{ch} values for both the ALD- and PVD-TiN gate FinFETs. Note that the slope (dR_{ch}/dL_g) of this plots is propotional to the invers of the mobility [9]. It is obvious that the slope for ALD case with L_g over 500 nm is steeper than that for PVD case. This indicates lower mobility for ALD case in long L_g region, which is consistent with the measured mobility data of Fig.5. However, the slope for ALD case with L_g below 500 nm is almost the same value as PVD case. This indicates that mobility of the ALD- and PVD-TiN is comparable in the shorter L_g region, because the gate induced stress is relaxed with L_g scaling [10]. Figure 9 shows Pelgrom plot of the ALD- and PVD-TiN gate FinFETs. It should be noted that σ_{Vth} is smaller for ALD case than that for PVD case. The reason for the smaller σ_{Vth} of the ALD-TiN case is discussed with regard to the TiN grain sizes. The crystalline structure of the ALD and PVD TiN is investigated using nano beam diffraction (NBD) pattern as shown in Fig.10. A hollow pattern resulting from an amorphous-like film can be observed in ALD TiN in contrast with PVD TiN. Thus the ALD-TiN gate has smaller grain size than that for the PVD-TiN gate. We consider small σ_{Vth} of the ALD TiN gate case is due to the small grain size of the ALD TiN case. To investigate this origin of the grain size differnce, we investigate the composition of the ALD- and PVD- TiN films obtained by XPS analysis, as shown in Fig 11. It was found that ALD TiN retains carbon impurity originated from dimethyamine. The carbon impurity suppresses the grain growth of ALD TiN, which leads to the smaller V_{th} variation of the ALD TiN gate FinFETs [11].

Conclusion

We have comparatively investigated the electrical characteristics including the mobility and the V_{th} variation of the fabricated ALD- and PVD-TiN gate FinFETs. The long channel mobility of electron is degraded by compressive stress of the ALD TiN. However mobility of the ALD- and PVD-TiN is comparable in shorter channel (L_g<500 nm), because the gate induced stress is relaxed with L_g scaling. The V_{th} variation of the ALD TiN is lower than that of PVD TiN thanks to the smaller grain size of the ALD TiN.

Acknowledgement

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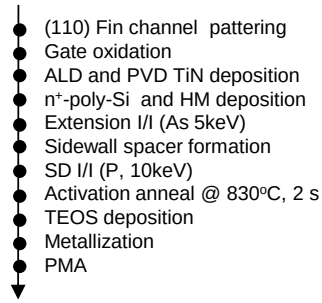

Fig. 1 Process flow of the TiN gate FinFETs.

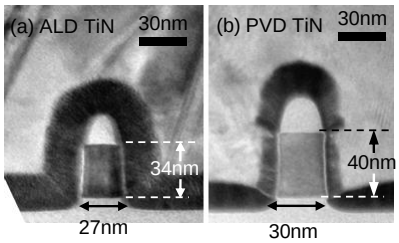

Fig. 2 Cross sectional TEM views of the fabricated (a)ALD- and (b)PVD-TiN gate FinFETs.

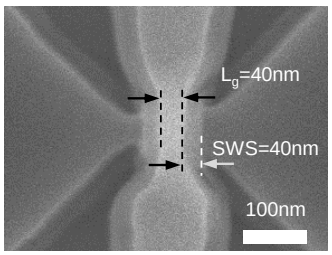

Fig. 3. SEM plane view of the fabricated FinFET with L_g = 40nm.

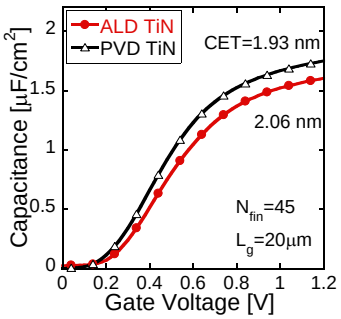

Fig. 4. Split-CV characteristics of the fabricated ALD- and PVD-TiN gate FinFETs.

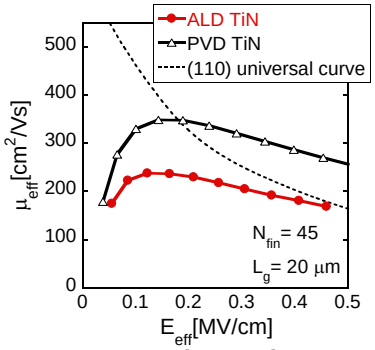

Fig. 5. Comparison between the measured electron mobility of the long channel multi FinFETs.

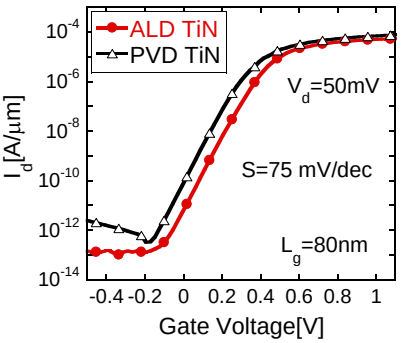

Fig.6. Typical I_d-V_g characteristics of the ALD- and PVD-TiN gate FinFETs with L_g = 80nm.

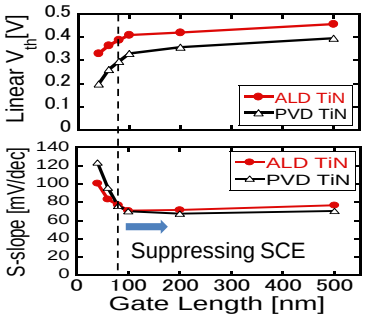

Fig.7. Measured V_{th} and S-slope of the fabricated FinFETs as a function of L_g.

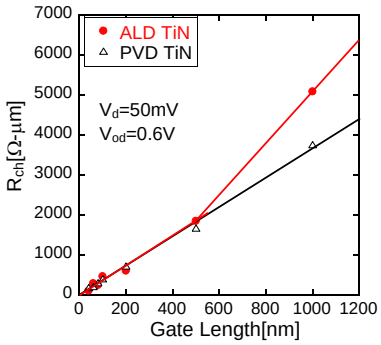

Fig. 8. R_{ch}-L_g plots of the fabricated ALD- and PVD-TiN gate FinFETs.

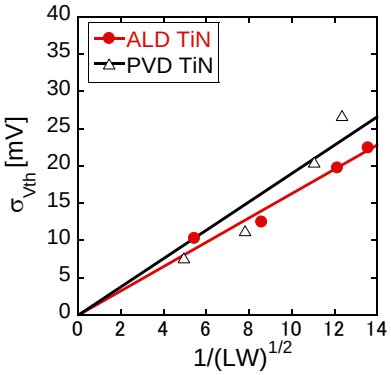

Fig. 9. Pelgrom plots of the fabricated ALD- and PVD-TiN gate FinFETs.

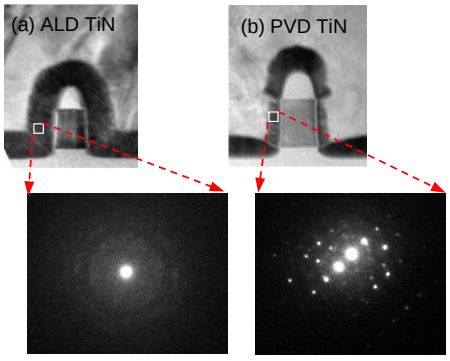

Fig.10. NBD pattern of the (a) ALD- and (b) PVD-TiN on the side of the fin channel.

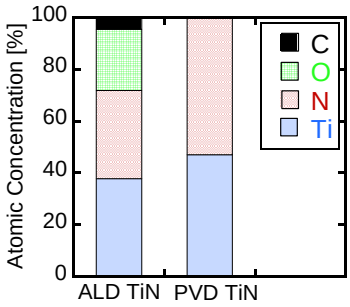

Fig.11. Composition of the ALD- and PVD-TiN films evaluated by XPS.