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Extremely scaled (~0.2 nm) equivalent oxide thickness of higher-k ALD-HfO_2 gate stacks

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1. Introduction

In equivalent oxide thickness (EOT) scaling for the sub-0.5-nm regime, the use of "higher-k" (k > 30) dielectrics is a promising solution for the reduction of gate leakage current (Jg). In this study, we demonstrate extremely scaled higher-k HfO_2 gate stacks. The HfO_2 layer is directly deposited on Si by atomic layer deposition (ALD) without a SiO_2 interfacial layer (IL). The dielectric constant of HfO_2 is enhanced to k = 40 by generating cubic crystallographic phase. [1,2] By using these fabrication techniques, extremely thin ~0.2 nm EOT was realized.

2. Experimental

The enhancement of the permittivity of the HfO_2 layer has already been proposed (cap-PDA technique, **Fig. 1**). [1,2] By using abrupt and short-time annealing with a TiN capping layer, amorphous HfO_2 crystallizes into the high-permittivity cubic phase. The X-ray diffraction (XRD) spectra before and after TiN cap-PDA clearly show that the amorphous phase transforms into the cubic phase [**Fig. 1(c) & (d)**]. However, the results of cross-sectional transmission electron microscopy (X-TEM) show that a thick SiO_2 IL grows simultaneously [**Fig. 1(a) & (b)**]. This is because the oxygen released from HfO_2 during crystallization oxidizes the Si substrate [**Fig. 2(a)**]. In order to suppress IL growth, we have developed a novel oxygen-controlled cap-PDA technique where Ti capping layer was used instead of TiN [**Fig. 2(b)**]. Ti can absorb up to 30 at% of oxygen without forming Ti oxide. [3] Then, it is expected that ~6 nm Ti capping layer can suppress ~2 nm of SiO_2 IL growth by absorbing excess O from HfO_2. **Fig. 3** shows the experimental setup. ALD HfO_2 was directly deposited on the OH-terminated Si surface to form a Si-O-Hf direct contact interface. [4] Ti and TiN were deposited as the capping layer and the gate electrode, respectively.

3. Direct-contact higher-k HfO_2 gate stacks

X-TEM images of the HfO_2 gate stacks show the effective suppression of the SiO_2 IL growth by Ti cap-PDA (**Fig. 4**). Secondary ion mass spectroscopy (SIMS) analysis shows the accumulation of O atoms in the TiN/Ti layer after Ti cap-PDA (**Fig. 5**). These O atoms are the residuals released from HfO_2. XRD spectra (**Fig. 6**) show the generation of the cubic phase (c-HfO_2) in 2.4 nm HfO_2 and the co-existence of the cubic and monoclinic phases (m-HfO_2) in 3.2 nm HfO_2. The plot of the C–V characteristics (**Fig. 7**) shows that the capacitance of the HfO_2 gate stacks increases as the HfO_2 thickness decreases. From the *C–V* curve for 2.4 nm HfO_2 nMOS, the 0.25 nm EOT was estimated. The analysis of the impedance–frequency (*Z–f*) measurements (**Fig. 8**) shows that the measured real and imaginary parts of the impedance agree with those obtained from the simulations. These results indicate the validity of the 0.25 nm EOT. In the relationship between HfO_2 thickness (T_{Phys}) and EOT (**Fig. 9**), a very thin EOT abruptly increases at around T_{Phys} = 2.6 nm. The dielectric constant (k) was estimated to be 40 below T_{Phys} = 2.6 nm and 18 above it. These values are consistent with those estimated from the X-TEM images. The extremely high dielectric constant around 40 possibly originated from the cubic phase. On the other hand, an appearance of monoclinic phase in thicker T_{Phys} obviously degraded the permittivity. (See **Fig. 6**) In the Jg–V and Jg–EOT plots (**Fig. 10 & 11**), Jg for the 0.28 nm EOT is large but shows an advantage over the trend for the k = 13 HfO_2 gate stacks in the very thin EOT region. [6] The Id–Vds curve of the nFET (**Fig. 12**) clearly shows inversion mode operation. The Id–Vgs curve of the 0.25 nm EOT (**Fig. 13**) shows the apparent on/off feature, but the large Id value expected from a very thin EOT was not obtained. The electron mobility seems to be severely degraded compared to the universal mobility, especially in a very thin EOT (**Fig. 14**). The insertion of a SiO_2 IL effectively recovers the mobility. However, for a sub-0.5-nm EOT, an IL thickness of up to 1 ML (~0.3 nm) can be permissible. Such an ultrathin IL would have no drastic effect on recovering the mobility. Control of the interface dipole, fixed charge reduction in high-k gate stacks and electrodes, and interface roughness reduction could be the residual efforts.

5. Conclusion

We demonstrated extremely scaled higher-k HfO_2 gate stacks by crystallization of ALD-HfO_2 and suppression of the SiO_2 IL. The dielectric constant of HfO_2 was enhanced to 40 and the EOT was decreased to as thin as ~0.2 nm. Mobility degradation will remain as a final issue of sub-0.5 nm EOT scaling.

Acknowledgements

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[2] Y. Morita, et al., IWDTF (2011) 23, accepted in JJAP.
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[5] Simulated by "MIRAI-ACCEPT," N. Yasuda, et al., SSDM (2005) 250.
[6] Y. Morita, et al., SSDM (2009) 52.

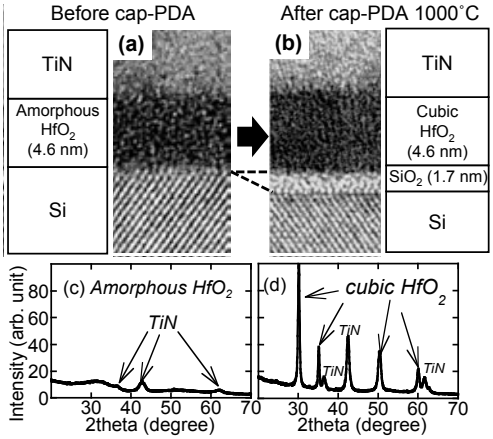

Fig. 1 Concept of permittivity enhancement in HfO_2 gate stacks by using the cap-PDA technique. (a) and (b) show X-TEM images of HfO_2 gate stacks before and after cap-PDA with a TiN capping layer, respectively. The gate stack structures are also shown. (c) and (d) show XRD spectra for TiN-capped HfO_2 before and after cap-PDA, respectively. By using abrupt and short-time annealing with a capping layer, amorphous HfO_2 crystallizes into the cubic phase. The dielectric constant of cubic HfO_2 is known to be ~50. [1] However, a SiO_2 IL grew simultaneously because of the oxygen released during crystallization.

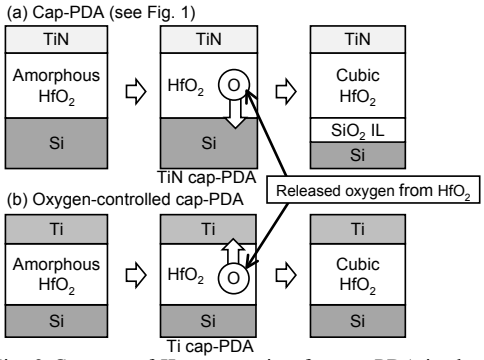

Fig. 2 Concept of IL suppression for cap-PDA in the present study. In (a), TiN hardly absorbs oxygen, and then, oxygen released from HfO_2 oxidizes Si. In (b), the novel oxygen-controlled cap-PDA uses a Ti capping layer, which has strong oxygen absorbability. Reduction of oxygen during PDA suppresses SiO_2 IL formation.

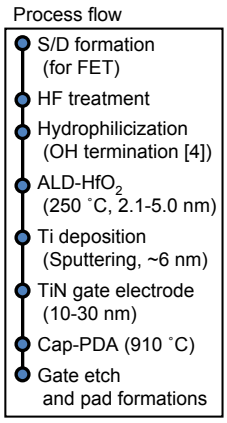

Fig. 3 Sample preparation procedure of this experiment. The HfO_2 layer was directly deposited on OH-terminated Si without a SiO_2 IL. Source and drain regions were preferentially formed for the gate last FET.

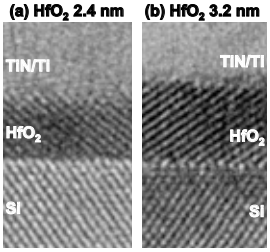

Fig. 4 X-TEM images of the TiN/Ti/ALD-HfO_2/Si gate stacks after cap-PDA at 910 °C. No SiO_2 IL is observed, and the HfO_2 layers crystallize in both the 2.4 and 3.2 nm cases. (See Fig. 6.)

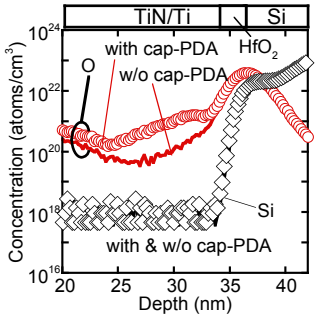

Fig. 5 Front-side SIMS of the TiN/Ti/ALD-HfO_2/Si stacks, confirming the accumulation of O and Si atoms in the TiN/Ti layers. The cap-PDA temperature was 910 °C. The O atoms in the TiN/Ti layers increased after cap-PDA.

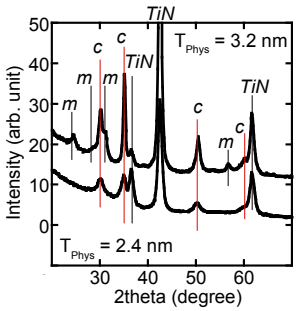

Fig. 6 In-plane XRD for 2.4 and 3.2 nm ALD HfO_2 after cap-PDA at 910 °C. The indexed c and m peaks indicate the cubic and monoclinic phases of HfO_2, respectively.

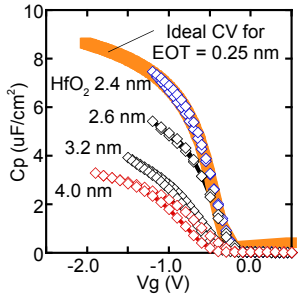

Fig. 7 *C–V* curves of TiN/Ti/ALD-HfO_2/Si nMOS gate capacitors. The data were frequency-corrected with 500 kHz and 1 MHz. The Ideal *C–V* curve is simulated by MIRAI-ACCEPT [5].

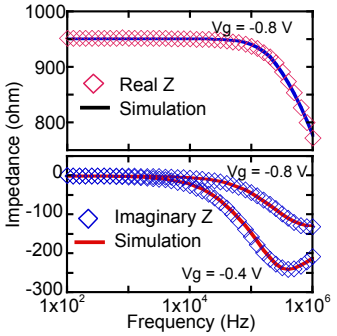

Fig. 8 *Z–f* measurements of TiN/Ti/ALD-HfO_2/Si gate stacks of 0.25 nm EOT. Simulated curves are also plotted on the basis of the three-component device model. The simulated curves agree with the measured *Z–f* values. This validates the 0.25 nm EOT in this experiment.

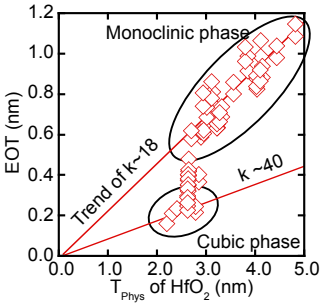

Fig. 9 *EOT–*T_{Phys} plot for the TiN/Ti/ALD-HfO_2/Si gate stacks. Two different trends of the dielectric constant can be recognized.

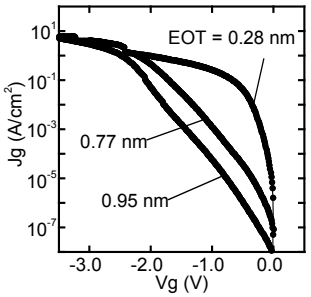

Fig. 10 J_g–V_g plot for the TiN/Ti/ALD-HfO_2/Si gate stacks.

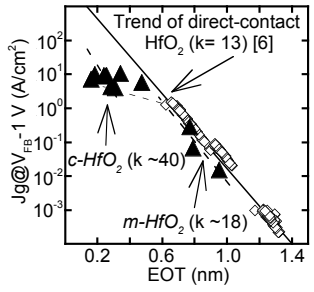

Fig. 11 J_g–*EOT* plot for the TiN/Ti/ALD-HfO_2/Si gate stacks. The trend of direct-contact HfO_2 gate stacks (k = 13) is also plotted for comparison.

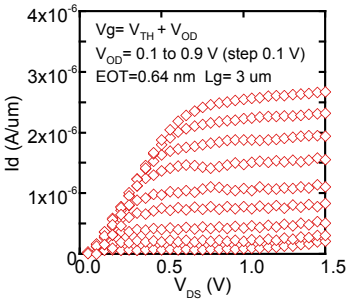

Fig. 12 I_d–V_{ds} characteristics of the TiN/Ti/ALD-HfO_2/Si nFET. Lg = 3 µm.

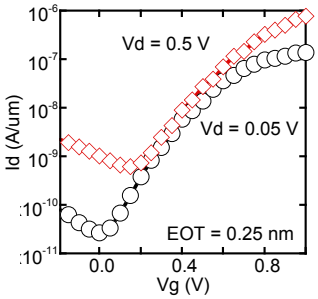

Fig. 13 I_d–V_g characteristics of the TiN/Ti/ALD-HfO_2/Si nFET. Lg = 3 µm. The I_d curves are deformed due to large leakage current on long channel FET.

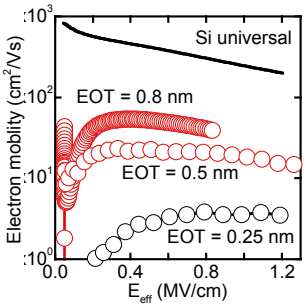

Fig. 14 Electron mobility of the TiN/Ti/ALD-HfO_2/Si nFET as a function of the effective field.