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Magnetoresistive Random Access Memory with Spin Transfer Torque Write (Spin RAM) - Present and Future -

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1. Introduction

Magnetoresistive random access memory using magnetic tunnel junction (MTJ), a nonvolatile spintronic device, as a key element combined with spin transfer torque (STT) write is capable of fast-read/write with high endurance together with good back-end-of-line (BEOL) compatibility. Recent progress in perpendicular magnetic-easy axis MTJs offers a high potential for constructing scalable stand-alone fast and nonvolatile RAMs in the 30 nm feature size and beyond. These high performance nonvolatile RAMs based on MTJ and its variants (hereafter called Spin RAM) can also be used in conventional VLSI circuits and systems as an embedded nonvolatile RAM. Moreover, it opens a route to nonvolatile CMOS logic employing logic-in-memory architecture. In the following, I review the current status of MTJ based Spin RAMs and discuss about the remaining challenges and future prospects.

2. Memory Hierarchy

In current microprocessor systems, there are performance gaps between the operating speeds of core, memory and storage. Figure 1 (a) illustrates the speed performance, circuit density and power consumption of layers in a current microprocessor system [1]. In order to keep up with the demand for higher processing throughput, it is necessary to decrease the speed gap between the core and other memories with minimum power penalty. Figure 1 (b) shows a system hierarchy with Spin RAM; using Spin RAM, the speed gap can be reduced considerably, with minimum power penalty or even reduction of power required for the same performance. By employing logic-in-memory architecture with high speed nonvolatile back-end compatible memory such as Spin RAM, a future system hierarchy with enhanced performance with further reduction of power can be envisaged as in Fig. 1 (c). Here, the logic and memory circuits are integrated taking advantage of the fact that those MTJ devices can be embedded in the interconnection layer. This configuration reduces the global delay time of the signal inside the circuit, static power to nearly zero, and the device count by integrating memory with logic.

3. MTJ Technology

A high performance MTJ needs to satisfy five requirements: (1) small size (F nm), (2) low current for current-induced magnetization switching ($I_{C0} \leq F$ μA), which is proportional to the product of magnetic damping parameter α and the energy barrier E that magnetization needs to overcome, (3) high tunnel magnetoresistance (TMR) ratio (>100%), where the ratio is defined as $(R_{AP}\text{-}R_P)/R_P$ using the resistance at parallel magnetization configuration (R_P) and the resistance at antiparallel configuration (R_{AP}) (4) high thermal stability factor of free layer $\Delta = E/k_BT$ (>40), which in ideal case is equal to the energy barrier that needs to be overcome by current, and finally (5) capability to withstand annealing temperature of 350 °C to 400 °C required for standard semiconductor processing. It has been shown that 40 nm perpendicular-MTJ (magnetization of the free and fixed layers is pointing perpendicular to the substrate) utilizing the perpendicular anisotropy at the interface of MgO-CoFeB can satisfy nearly all the requirements [2]. The CoFeB-MgO-CoFeB MTJ shown in Fig. 10 satisfies all the requirements at the diameter as low as 40 nm, except for the switching current (49 μA), which is higher than preferred 40 μA or less. In order further to advance the technology, one needs to simultaneously increase Δ and reduce I_{C0}. By developing material technology to increase the interface anisotropy and to decrease α, high performance 30 nm MTJ and beyond will be in sight.

4. Nonvolatile spin RAM

Following the seminal work on 4 kbit spin RAM [3], a number of groups have demonstrated higher capacity of Spin RAM year by year [4], reaching 64 Mbit in the year 2010 [5].

There are two directions to go. One is to develop Spin RAM that replaces standalone DRAM [6, 7]. To this end, one needs to develop a very high density RAM, preferably more than 1 Gbit, meaning small feature size with sufficient Δ. Developing processing technology, particularly etching of metal stacks, is another challenges in this direction. The 350 to 400 °C annealing requirement might not as stringent for this direction, because one can optimize the entire process flow to be compatible with the available MTJ technology.

The second direction is to develop an embedded DRAM/SRAM replacement. Here, the 350 to 400 ^{o}C annealing is an absolute must, because one cannot change the optimized CMOS logic part. The feature size is not as big a requirement as in the standalone DRAM replacement, however, particularly for the SRAM replacement. This is due to the fact that the current SRAM is already using 150 F^2 or more area. It has been shown that one can increase the stability of an MTJ by making the hard layer size greater than that of the free layer. For very high speed operation, a 3-terminal spin device that separates the write path from the read path is another possibility. Recently 16 kbit content addressable memory with 5 ns search time has been developed using 3-terminal domain wall spin device [8]. Nonvolatile logic-in-memory architecture is a natural extension of this direction. Here the latest development is the 6T-2MTJ nonvolatile 2 kbit ternary content addressable memory that can reduce search mode power to 1/30 of the comparable CMOS realization [9].

4. Challenges and Prospects

The scalability of Spin RAM will be determined by both materials and process integration development. It is a big challenge and is difficult to predict how far in dimension one can go at this point. One thing that can be pointed out is that the spintronics nonvolatile memory approach has solid grounds in terms of science and technology; there is an established magnetism and magnetic materials science base together with a large hard disk drive industry. We can certainly learn a lot from the materials science for hard disk media that can realize high Δ at dimensions less than 10nm

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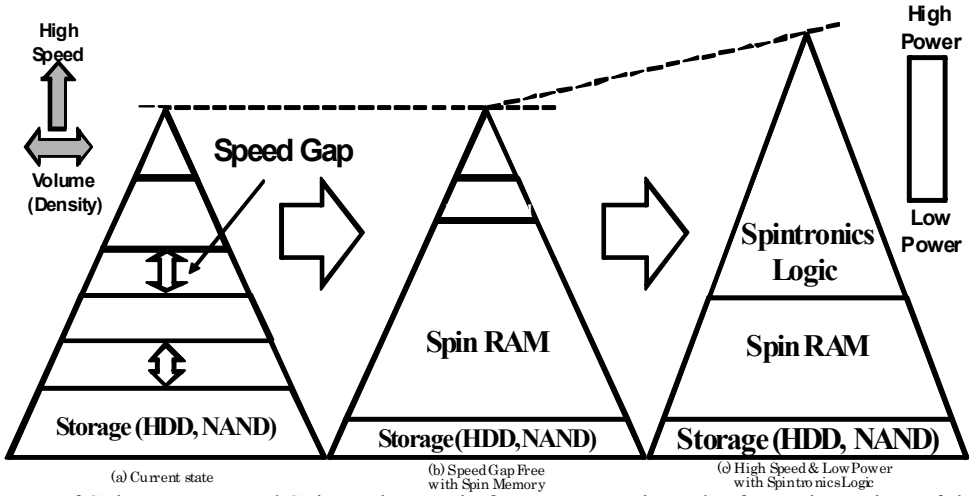

Figure 1 Impact of Spin Memory and Spintronics Logic for Memory Hierarchy from viewpoints of the speed performance, circuit density and power consumption. After ref. [1]

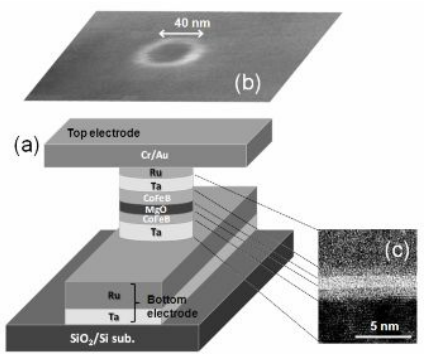

Figure 2 Perpendicular easy axis MTJ that utilizes interface perpendicular anisotropy at the interface between MgO and CoFeB. This 40 nmϕ MTJ can be annealed at 350 ^{o}C with the resulting switching current of 48 μA and TMR ratio of 110%. Δ was approximately 40. [1]