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Studies on Static Noise Margin and Scalability for Low-Power and High-Density Nonvolatile SRAM using Spin -Transfer -Torque (STT) MTJs

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1. Introduction

To suppress the ever-increasing leak power in highly scaled LSIs, NV logic circuits and memories are indispensable [1]. MTJ with STT switching mechanism (STT-MTJ) can be used to achieve this goal because of its scalability, high-speed operation and virtually unlimited write endurance [2]. If a small and large-signal NV SRAM cell is used in large scale embedded memories, its impact on the chip's power reduction is enormous by ultimate power management realizing its nonvolatility. In this paper, we propose a novel STT-SRAM cell whose static noise margin (SNM) is enhanced by the MTJ switching and show its good scalability with cell size smaller than the 6T SRAM cell.

2. Cell Operation

The proposed STT-SRAM cell has a simple structure in which the resistors in the resistive load SRAM cell are replaced by MTJs as is shown in Fig. 1. It is essential that the pinned layers in the MTJs are connected to power line V_{PL}. Fig. 2 is the DC SPICE simulation results in 32nm node indicating that data are held at a pair of storage nodes SN and /SN for the cell in Fig. 1. It also indicates that the data is not retained at the nodes if the MTJs are connected in the opposite direction, because the Anti-Parallel (AP) state of the MTJ is flipped to the Parallel (P) state due to the large disturb current for V_{dd}≥0.7V. We used SPICE with an MTJ model implemented whose parameters are fitted to measurement results. Fig. 3 illustrates a two-step write sequence where the AP state is written in the first step followed by the P state. Though the power is off prior to read, the data stored in the MTJs are immediately latched by powering-on the cell for read as is shown in Fig. 2. The retention power is totally eliminated by setting V_{PL} to GND.

3. Static Noise Margin

The stable operation of the proposed STT-SRAM is verified by measuring V-I characteristics of the MTJ whose cross-sectional TEM view is shown in Fig. 4. Fig. 5 is the measured V-I curves for the MTJ of size 100nmx200nm with the free layer grounded and the voltage applied to the pinned layer. The data represent load curves of the inverter comprising the STT-SRAM and they are combined with nFET V_d-I_d driver curves with V_g changed for W/L_g=3μm/0.14μm to obtain the inverter DC characteristics as shown in Fig. 6. The MTJ switching from R_P to R_{AP} is observed at about V_{IN}=0.7V. The resultant SNM curves are shown in Fig. 7 (a) for the state "0" where a lower voltage is held at the node SN and Fig. 7 (b) for the opposite state "1". The MTJ switching is understood to be the origin of the SNM improvement as shown by the solid arrows. In the graphs, the SNM of the resistive load SRAM cell is added with resistors of 1.2KΩ that is roughly $(R_P+R_{AP})/2$. The SNM of the STT-SRAM cell is 0.34V and is 25% larger than that of the resistive load SRAM cell (0.27V) owing to the resistance self-adjustment to changing the trip points of the inverters for enhancing the SNM.

4. Cell Size Scaling

One concern for the STT-SRAM cell is its cell size. Because a current of several hundreds of microampere is required for changing the state of the MTJ around the size 100nm diameter, the FET channel width needs to be about a micrometer to supply the current for L_g=100nm. However, since the write current is experimentally shown to reduce as the size of the STT-MTJ shrinks, it is expected that the cell becomes smaller in the future by reducing the MTJ size. Furthermore, we experimentally show the resistance-area product *RA* of the MTJ as a function of MgO (tunnel barrier) thickness in Fig. 8. It indicates that *RA* depends exponentially on the thickness, implying that further cell size reduction can be realized by thinning the MgO thickness along with the MTJ size shrink, because the thinning can suppress the resistance increase due to the size shrink. Fig. 9 shows trends of the minimum channel widths of the nFETs applicable in the STT-SRAM cell that are estimated from measured MTJ performances with V_{dd} kept at 1V. The write current is assumed to reduce in proportion to the MTJ size. We consider three scaling scenarios for MgO thickness according to Fig. 8: (1) a main scenario: thinning from 1.1nm to 0.8nm (*RA*: from 7.85 to 3.04 Ωμm^2), (2) a reference scenario: without thinning at 1.1nm (*RA*=7.85Ωμm^2), (3) another reference scenario: thinning from 1.1nm to 0.5nm corresponding to a constant resistance (*RA*: from 7.85 to 0.23 Ωμm^2). 100% MR ratio is assumed. Since $W=2L_g$ is a typical channel width of the FETs used in the 6T SRAM cell, the STT-SRAM cell size can catch up the 6T SRAM cell for 45nm (L_g=50nm) node for the scenario (1). Fig. 10 illustrates a layout of the STT-SRAM cell at 45nm node and beyond for the scenario (1). The cell size is 91F^2 that is 42% smaller than the 6T SRAM counterpart [3]. The smaller cell size is realized by placing the MTJs on the FETs and the wirings as shown in Fig. 11.

5. Conclusions

We propose a novel STT-SRAM cell to show that its SNM is enhanced by 25% due to the MTJ switching. It is estimated that the MTJ size and its MgO thickness scaling can contribute to reduce its cell size down to the 6T SRAM cell size and smaller.

Acknowledgements

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References

[1] T. Hanyu et al., *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers,* p. 208, 2002. [2] S. Ikeda et al., *IEEE Trans. Electron*

Devices, vol. 54, p. 991, 2007. [3] S. Ohbayashi et al., *IEEE J. Solid-State Circuits*, vol. 42, p. 820, 2007.

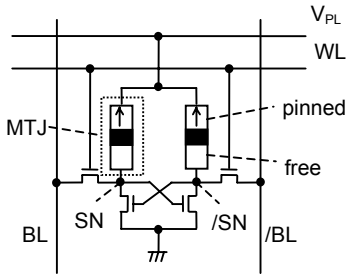

Fig. 1 Schematic of the STT-SRAM cell consisting of 4 N-type MOSFETs and 2 MTJs.

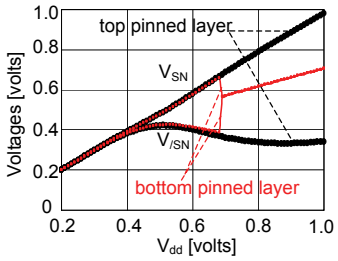

Fig. 2 DC analysis for data hold for the cell with top pinned layers (see Fig. 1) and bottom pinned layer.

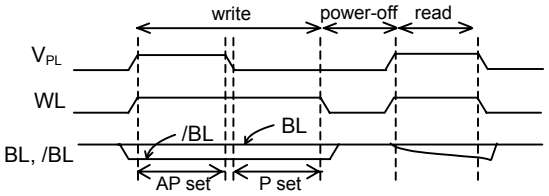

Fig. 3 Operational waveforms for write and read of the STT-SRAM cell in Fig. 1. After power-off, no reload operation is needed to read the data.

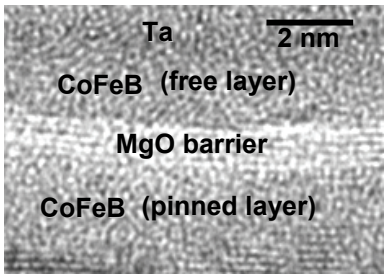

Fig. 4 Cross-sectional TEM image of the measured CoFeB-MgO MTJ.

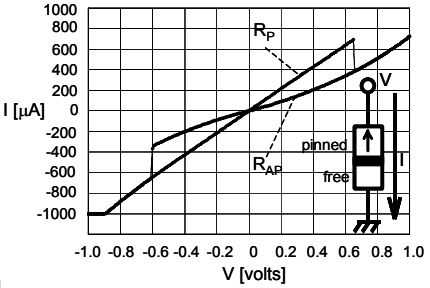

Fig. 5 Measured V-I characteristics of the MTJ of Fig. 4 the size of 100nmx200nm. R_P and R_{AP} are the resistances of MTJ in case of P state and AP state, respectively.

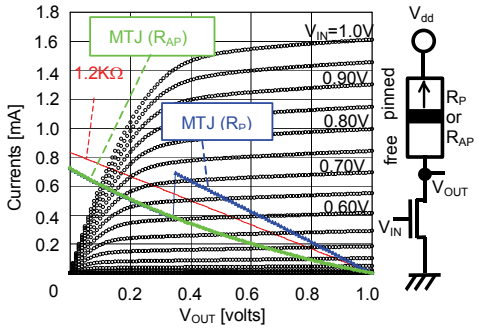

Fig. 6 Measured V-I characteristics of the MTJ in Fig. 5 is combined with I_d-V_d (V_g: parameter) characteristics for NFET with W/L=3μm/0.14μm. The load line for 1.2KΩ linear resistance is also added.

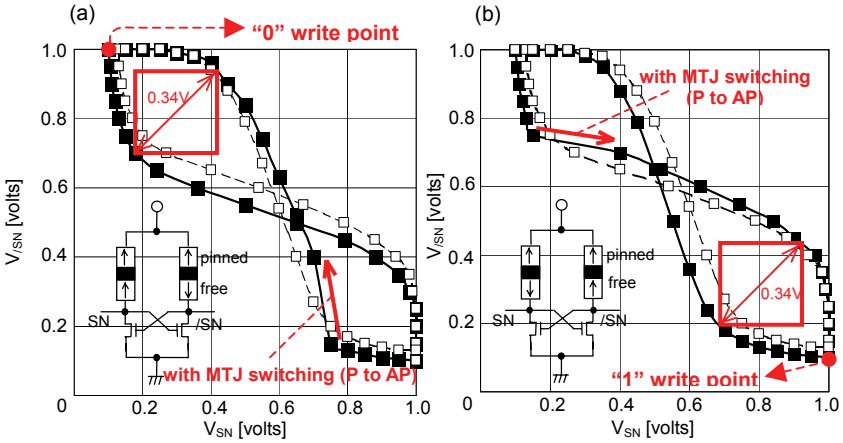

Fig. 7 SNM of the STT-SRAM cell (solid line) compared with that of the resistant load SRAM cell (broken line).

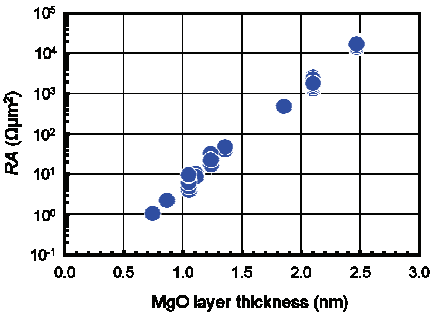

Fig. 8 Measured resistance-area product as a function of MgO thickness.

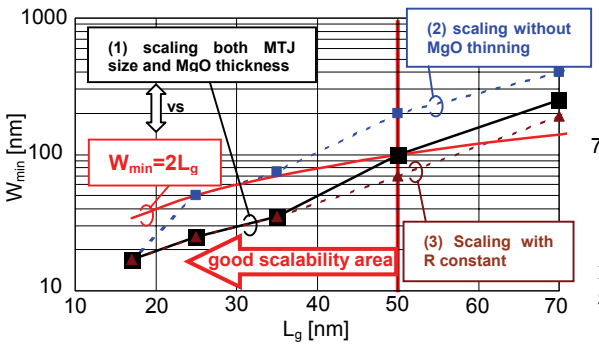

Fig. 9 Scaling trend of the channel width minimum for the STT-SRAM cells from 70nm to 16nm generations.

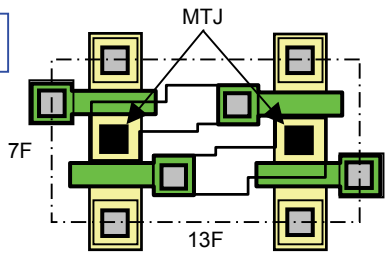

Fig. 10 Layout for the STT-SRAM cell for 45nm generation and beyond in the scaling scenario (1).

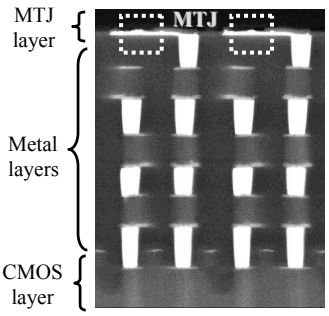

Fig. 11 Cross-sectional SEM image of MTJs placed on CMOS and metal wires.