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A Study for Adopting PMOS Memory Cell for 1T1R STT-RAM with Asymmetric Switching Current MTJ

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1. Introduction

Spin Transfer Torque RAM (STT-RAM) using Magnetic Tunnel Junction (MTJ) thin films[1] is one of the most promising nonvolatile memory candidates because of its low voltage, high speed and high write endurance features[2]. In order to realize an STT-RAM with a large capacity, it is desirable to adopt a 1T1R memory cell, which consists of 1-transister and 1-MTJ. However, when a 1T1R memory cell is used for an STT-RAM, there is a problem that lowers the write margin of the STT-RAM. Reference [3] reports that it comes from the asymmetric switching current of the MTJ, that the value of write current is different depending on the direction of the current. This paper will discuss the problem and its solution, from the viewpoint of achieving large capacity STT-RAM.

2. Asymmetric Switching Current of MTJ

Figure 1 shows the diagram of a 1T1R memory cell. As is well known, an MTJ device has the stack structure, which includes Free layer, MgO layer and Pinned layer. In the case when the magnetization direction of the Free layer is parallel or anti-parallel to that of the Pinned layer, the resistance between the Free layer and the Pinned layer is Rp or Rap (Rp<Rap), respectively. To avoid process difficulties, the Pinned layer is usually formed physically underneath the Free layer.

Figure 2 illustrates current vs. resistance characteristics for a typical MTJ device. In data write operation, the Rap state can be flipped to the Rp state by applying the current flow to be more than Iw0 toward the Forward Current direction shown in Fig. 1 and 2. Conversely, the Rp state can be flipped to the Rap state by applying the current flow to be more than Iw1 toward the Reverse Current direction.

Reference [3] describes the following relationship between Iw0 and Iw1,

$$\frac{Iw1}{Iw0} = \frac{1 + P_0^2}{1 - P_0^2} \quad , \qquad (1)$$

where P_0 is the first order approximation of the tunneling spin polarization. The right side of the equation (1) is obviously more than 1, thus Iw1 > Iw0. This fact is called the asymmetry of the write (switching) current.

In the memory cell transistor operation, in order to apply the Forward Current, the word line (WL) is set at the supply voltage (VDD), the bit line (BL) is set at the VDD, and the source line (SL) is set at the ground (GND). The simulated waveforms for the operation are shown in Fig. 3. The gate-source voltage Vgs of the transistor is VDD in this case. On the other hand, to apply the Reverse Current, the BL is set at the GND and the SL is set at the VDD. In this case, the voltage of the cell node (CN), which acts as the source of the transistor, becomes higher than the GND level. Hence the Vgs of the transistor is VDD - the voltage of CN. This causes the Reverse Current to the MTJ to be smaller than the Forward Current in the memory cell operation. That is, the current drivability of the transistor is degraded in the 1T1R memory cell operation, in spite of the MTJ requiring a larger current for the Reverse write and a smaller current for the Forward write.

3. Introducing PMOS memory cell transistor

To solve the above problem, there are some techniques as follows. First, using a local wiring in the memory cell, the drain terminal of the transistor is connected to the top electrode (Free layer), and the BL is connected to the bottom electrode (Pin layer). This solution, however, costs in having a 1.5 ~ 2 times larger memory cell size. Second, reference [6] reports the device technology, which reverses the direction of Iw1 by making the Pinned layer to the top electrode. But this structure might be hard to manufacture, especially for the perpendicular MTJ[1], which will be the mainstream in the future scaled device.

We regard the PMOS memory cell transistor shown in Fig. 4 as a promising solution, because the Vgs loss by BL and SL voltage is opposite to the NMOS case. As shown in Fig. 5(a), for NMOS transistor, write is performed using the less On current Ion0 against Iw0 of MTJ. Also, it is wasteful that Ion1 (> Ion0) is used for Iw1 (<Iw0) writing. By using PMOS transistor, the magnitude correlation between Iw0, Iw1 and Ion0, Ion1 matches well (Fig. 5(b)), resulting in achieving an efficient write operation.

However, the On current for PMOS transistor is usually about a half of that for NMOS transistor, a careful attention to avoid write current shortage must be paid. Here, using SPICE simulation, the above solutions are compared: (1) NMOS + BL Free layer (conventional), (2) NMOS + BL Pinned layer (memory cell local wiring or top Pinned layer structure[6]), (3) PMOS + BL Free layer (proposed). The condition used in the simulation is listed in Table 1.

Figure 6 shows the Forward/Reverse current drivability for each (1) ~ (3) case. Figure 6 also depicts write current values Iw0, Iw1 listed in Table 1, which are assumed for a typical perpendicular MTJ. Case (1) is incapable of Reverse Current write for the assumed Iw1. Case (2) and (3) are both OK, but the current value of (3) is less than that of (2).

Another parameter which characterizes MTJ is MR ratio. The MR ratio influences read operational margin for STT-RAM. The larger MR ratio value is, the better margin can be obtained. However, from the viewpoint of write operation, a large MR ratio means a high Rap resistance, thus too large MR ratio causes a malfunction due to write current shortage. Figure 7(a) shows the relations between the write current for anti-parallel to parallel (Iw0) and the allowed maximum MR ratio (MRmax) for Case (2) and (3). Case (3) is rather worse than Case (2).

To boost the PMOS gate terminal down to a slightly negative level when activated will improve the write margin as shown in Fig. 7(a). Figure 7(b) is the simulated result for the case that the WL (=PMOS gate) is set at -0.2 V. As understood in Fig. 7(b), -0.2 V voltage boost can enlarge the allowed Iw0-MRratio area of PMOS transistor, resulting in equalizing to the allowed Iw0-MRratio area of NMOS transistor. The WL voltage of about -0.2 V hardly degrades the reliability of memory cell transistors.

To apply -0.2 V to the WL, we designed the circuit, WL slightly negative voltage booster (WSNVB) circuit, as shown in Fig. 8. This circuit uses the gate capacitance coupling to the WL via PMOS Cw in the WL driver. By calculation, Cw transistor requires several μm of gate width

for 256 cells/WL, whose occupied area is negligible. The simulated waveforms are shown in Fig. 9.

Finally, the comparison between (2) and (3) is summarized in Table 2. The PMOS memory cell transistor with WSNVB achieves the equal operation margin as the NMOS transistor.

4. Conclusion

The problem in 1T1R STT-RAM write operation originated from asymmetric switching current of MTJ has been analyzed in detail. Write characteristics equal to NMOS memory cell transistor can be achieved without any sacrifices of cell area and/or process easiness, by using PMOS transistor together with the newly proposed WL slightly negative voltage booster circuit.

Acknowledgement

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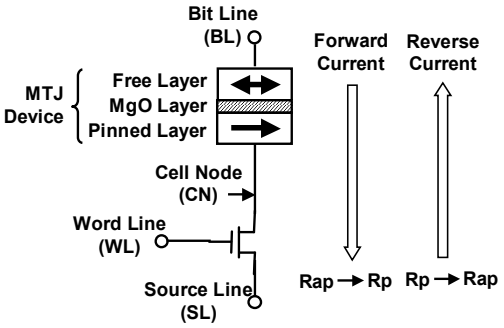

Fig. 1. 1T1R memory cell.

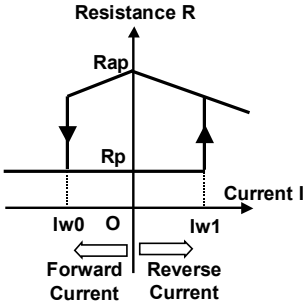

Fig. 2. Current vs. resistance for MTJ.

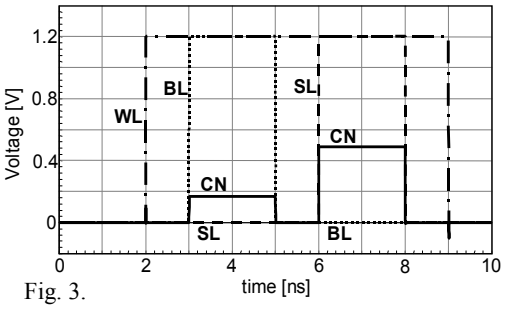

Fig. 3. Simulated waveforms for Forward/Reverse write. Predictive technology model [4,5] was used.

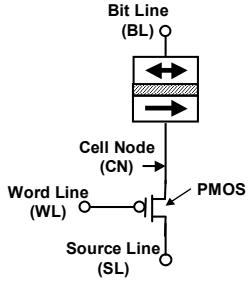

Fig. 4. PMOS memory cell transistor.

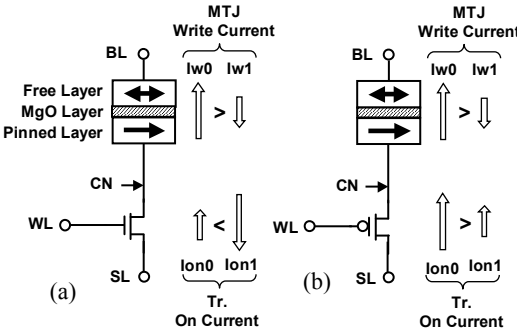

Fig. 5. Write operation for (a) NMOS transistor and (b) PMOS transistor.

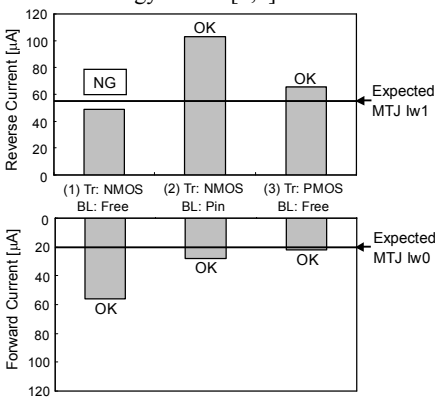

Fig. 6. Forward/Reverse current drivablity.

Table 1. Conditions used in simulation.

Transistor	
SPICE Model	Predictive Technology Model 90-nm CMOS [4,5]
Dimension	L=0.1μm, W=Wmin (Minimum Transistor Size for 90-nm CMOS)
MTJ	
Main Characteristics	Rp=10KΩ, MR=100%, Iw0=20μA, Iw1=55μA

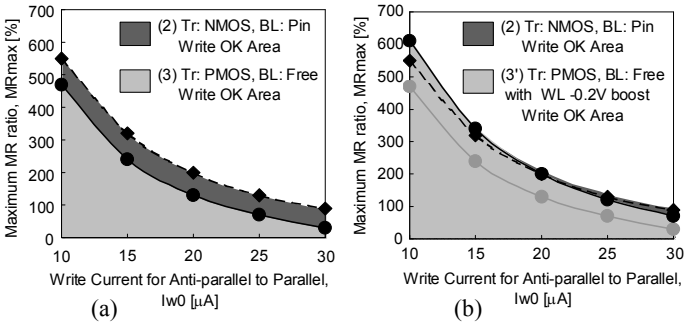

Fig. 7. Write current Iw0 vs. maximum MR ratio (a) Normal case (b) WL -0.2 V boost case

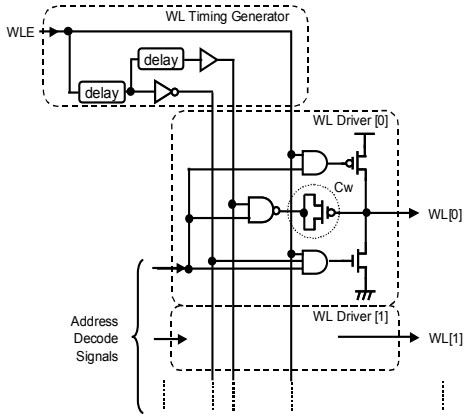

Fig. 8. Circuit diagram of WSNVB.

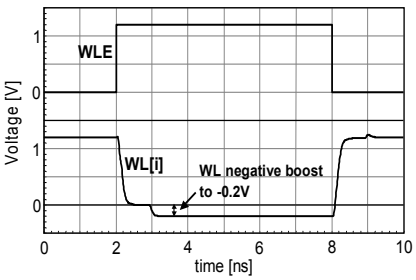

Fig. 9. Simulated waveforms of WSNVB.

Table 2. Comparison between NMOS and PMOS cell transistor.

	Technology	Cell Area	Process Easiness	Circuit Operational Margin
(2)	NMOS Tr + Local Wiring	Poor (x1.5 - 2)	Good	Good
(2)	NMOS Tr + Top Pin Structure	Good	Poor (Difficulty in Preparing MTJ)	Good
(3)	PMOS Tr + Bottom Pin Structure	Good	Good	Good (with WSNVB)