Novel 2step Writing Method for STT-RAM to Improve Switching Probability and Write Speed

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1. Introduction
Recently, as the result of aggressive scaling, conventional working memories, such as SRAM or DRAM, face big issues for the scaling. Moreover, for realizing low power system, nonvolatile working memory is required. Spin Transfer Torque RAM (STT-RAM) is one of the candidates because of its good performance: nonvolatility, high-speed operation, scalability, and excellent endurance [1]. However, STT-RAM has the issue of its switching probability in write operation under sub-10nsec [2]. In the case of conventional writing method using a single pulse, large write current is required for improving the switching probability [3]. This large write current requires a large cell size with a wide channel width cell MOSFETs, and induces large power consumption operation with high operation voltage, as well as a degradation of STT-RAM’s reliability etc.

In order to overcome these issues, we have proposed a novel 2step writing method for low power consumption of STT-RAM[4]. In this paper, we demonstrate experimentally the improvement of switching probability and write speed with proposed 2step writing method. Moreover, we developed the 2step pulse generation circuit.

2. Concept of 2step Writing Method for STT-RAM
Concept of 2step writing method for STT-RAM is shown in Fig.1. In this method, a base pulse is applied before a switching pulse input in write operation as shown in (b1). By applying the base voltage, initial energy, just before applying the switching voltage, is raised. The effective energy barrier of $\phi_2$ (see (b2)) in 2step writing method becomes smaller than $\phi_1$ (see (a1)) in the conventional method. Therefore, Energy margin for switching as shown in (b2) is enlarged. This is origin of improvement for switching probability and switching speed.

3. Switching Performance of STT-RAM with 2step Writing Method
Switching probability of 2step writing method is evaluated. Figure 2 shows the TEM image of the fabricated CoFeB/MgO/CoFeB based in-plane type Magnetic Tunnel Junction (MTJ). The measured MTJ is fabricated on 4-metal CMOS LSI and the junction size is $100 \times 200$ nm².

The applied base pulse and switching pulse are both 10nsec in width. Figure 3 shows an example of the observed waveform switched from an anti-parallel state ($R_{AP}$) to a parallel state ($R_p$). The base pulse voltage and the switching pulse voltage were changed as parameters. Pulse application measurement is performed 10 times for each 1-write ($R_0$ to $R_{AP}$) and 0-write ($R_{AP}$ to $R_0$).

Figure 4 shows the switching probability transition of the MTJ by changing the switching voltage. The black line shows the result of conventional writing method, and red line shows that of proposed 2 step writing method (base voltage $V_b$=0.6V). By proposed method, switching probability of 1-write improve by about 20% without raising the switching pulse voltage. Figure 5 shows switching time of the MTJ. Here, the switching time is defined as the time delay from the initial rise of output current pulse during switching pulse input to the switching. As shown in Fig.5, in cases of both 1-write and 0-write, switching time is reduced by the proposed 2step writing method. The switching time of 1-write is improved by about 40%. In order to evaluate effects of proposed writing method, energy assists with applying base pulse was estimated by using thermal activation model [5] in case of 1-write. As shown in Fig.6, the switching probability measured at 300K with conventional method and proposed method can be fitted by thermal activation model with temperature of 300K and 400K, respectively. From this result, it is estimated that by applying the base voltage of 0.6V, effective energy barrier $\phi$ is reduced by 100K.

It is experimentally verified that the switching probability and the writing speed of STT-RAM are improved by our proposed 2step writing method.

4. High-speed 2step Current Generator
We designed and fabricated the high-speed 2step current pulse generator by 90nm CMOS process as shown in Fig.7. Figure 8 shows its block diagram. As shown in Fig.9, the fabricated current generator can successfully generate the switching pulse in width from 450psec to 2.8nsec after generating the base current pulse.

5. Conclusions
It is experimentally demonstrated that the switching probability and switching speed of STT-RAM can be improved by proposed 2step writing method. In the case of 1-write of $V_b$=0.6V, switching probability was improved about 20% without raising switching pulse voltage. Moreover, we developed 2step pulse current generator with 90nm CMOS process that can successfully generate proposed 2 step current pulse with switching pulse of 450psec.

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References
Here, effective energy barrier of writing method. (a1) and (b2) shows band diagram just before switching pulse input. (a2) and (b1) shows electrons of the free layer just before switching pulse input and the top level of energy band of MTJ.

Here, the switching time is defined as the time delay from the initial rise of output waveform. Here, effective energy barrier of $\phi_1$ and $\phi_2$ is defined as the energy difference between electrons of the free layer just before switching pulse input and the top level of energy band of MTJ.

Fig. 5 Improvement of switching time by proposed 2-step writing method (a) 1-write (R\textsubscript{p} to R\textsubscript{AP}) (b) 0-write (R\textsubscript{AP} to R\textsubscript{p})

Fig. 6 Effects of applying base voltage in 1-write. Each measurement switching probability can be fitted by thermal activation model with $E_0/k_BT$ at 300K or 400K, respectively.

Fig. 8 Block diagram of designed over 1GHz high-speed current pulse generator. After inputting some configuration by command input, by inputting only trigger signal IN, 2-step pulse current is outputted.