Assessment of Erase-Verify Function in NAND Arrays with Charge-Based Capacitance Measurement


Abstract

To accurately assess the reverse read function during erase verification (EV) in NAND products, a test structure of a NAND string accompanied with a charge-based capacitance measurement (CBCM) circuit is employed. The relationship between bit-line flipping voltage (V\textsubscript{BL,f}) and reverse read bias (V\textsubscript{REV}) is then established. The impact of erase threshold voltage (V\textsubscript{T}) distribution is also evaluated. Furthermore, this methodology is validated as the result of this test structure is consistent with that of a functional product.

Introduction

A typical operation window of a floating gate (FG) NAND flash product is schematically depicted in Fig. 1. The horizontal axis means the V\textsubscript{T} of array cells while the vertical one represents the cell numbers located at each V\textsubscript{T} state. The width of V\textsubscript{T} at program/erase (P/E) states usually depends on process uniformity [1,2,3] and P/E algorithms [4]. Using the ground voltage as the read bias brings lots of benefits, and this implies that the V\textsubscript{T} of erased cells will be lower than 0V. For reliability considerations, such as charge loss [5] and read/program disturbances [6,7], sufficient read “0” and “1” margins (R0/R1) should be kept to reduce the risk of read errors. Thus, the V\textsubscript{T} of “0”/“1” state should be placed higher/lower than program/erase verification level (PV/EV).

To open the program distribution, verification of “0” state bit-by-bit is necessary, and Fig 2(a) exhibits how it works during program. A specific PV bias is applied on the word-line (WL) of the programming bit, and meanwhile, WLs of other cells (V\textsubscript{pass,read}) are kept high enough to sustain a conducting path. As described in literature [8,9], the V\textsubscript{T} judgment of a NAND string relies on the charge of string current. Once V\textsubscript{T} of the selected cell is higher than PV, the string current will be low enough, and then the program operation is finished.

Since over-erasure is not an issue for sensing in NAND, bit-by-bit verification is not suggested for accelerating erase operation. It is straightforward to apply a negative bias on all WLs within the string, and the erase operation is done when the string current is high enough. However, it will complicate the circuit design since an additional WL bias range is required. That is why a reverse read scheme as shown in Fig.2 (b) is usually adopted. Firstly, all WLs are biased at 0V as ~2V is applied on the common source line (V\textsubscript{CSL}). V\textsubscript{T} of cells is thus affected by body effect and becomes less easy to turn on. The bit line voltage (V\textsubscript{BL}) will be charged up if V\textsubscript{T} of all cells within the string has been low enough. Implementation of reverse read raises two major concerns: where the flipping V\textsubscript{BL} should be designed and how much R1 margin can be guaranteed. In this study, a specially-designed test structure is proposed to characterize the reverse read scheme in more detail.

Test Structure and Extraction Algorithm

Fig. 3 depicts the test structure. A NAND string comprising 12-cells of 70nm technology node is connected to a CBCM circuit. The circuit consists of one CMOS inverter for charging/discharging the V\textsubscript{BL}, and one PMOS capacitor of large area for storing the charges temporarily. All MOSFET features are listed in Table. 1. To achieve better measurement sensitivity, the loading capacitance (C\textsubscript{L}) herein is designed to match BL capacitance. The value of C\textsubscript{L} can be extracted by a two-step measurement. Waveforms during measurement are shown in Fig. 4. To isolate the influence of NAND string, string/group select transistors (SSL/SL) are always cut off. By using the properties of CMOS inverter, the V\textsubscript{BL} will be alternatively charged to V\textsubscript{DD} and discharged to ground by PMOS and NMOS respectively along with the waveform transition. The current which flows through PMOS (I\textsubscript{P}) is then recorded. C\textsubscript{L} can be expressed as,

\[ C\textsubscript{L}=I\textsubscript{P} \times T\textsubscript{period} / V\textsubscript{DD} \]  \hspace{1cm} (1)

T\textsubscript{period} means the period of charging time. It should be noted that the driving current or the charging period of PMOS should be large or long enough to ensure the capacitor is fully charged. Fig. 5(a) and 5(b) illustrate that a stable C\textsubscript{L}~2pF can be extracted once a suitable V\textsubscript{DD}, T\textsubscript{period}, or V\textsubscript{CP} is chosen.

V\textsubscript{BL} during EV can be obtained by using a similar concept and the corresponding waveforms are plotted in Fig. 6. At first, pre-charge of reverse read is performed by turning off CMOS inverter and C\textsubscript{L} is charged to V\textsubscript{BL} only by the current through NAND string. Then, NMOS of the inverter is turned on to create a discharge path. The resulting V\textsubscript{BL} can be written as,

\[ V\textsubscript{BL}=I\textsubscript{P} \times T\textsubscript{period} / C\textsubscript{L} \]  \hspace{1cm} (2)

As PMOS capacitor can be fully charged (by applying V\textsubscript{REV} high enough, 2V for example) to saturate at V\textsubscript{CSL}, deficient NMOS discharge timing will derive to wrong V\textsubscript{BL} due to smaller NMOS current (I\textsubscript{N}) being extracted. In Fig. 7(a), a stable V\textsubscript{N}L, equivalent to V\textsubscript{CSL} can be obtained, which suggests that NMOS can discharge the V\textsubscript{BL} normally when NMOS pulse width=0.1µs~1µs. Under a fixed width=200ns, the relationship between V\textsubscript{REV} and V\textsubscript{BL} is shown in Fig. 7(b). Acquiring V\textsubscript{BL} separates away from V\textsubscript{CSL} with decreasing V\textsubscript{REV}, at which V\textsubscript{BL} is limited by insufficient string current.

Owing to cells within a NAND string are serial connected, the cell with highest V\textsubscript{T} inevitably dominates the string current and thus limits the value of charged V\textsubscript{BL}. In other words, the V\textsubscript{T} distribution width of erased cells will affect the R1 margin. To quantitatively emulate such an effect, the V\textsubscript{T} within our test string is carefully controlled and divided into two groups as depicted in Fig. 8(a). Except the 6th WL (WL6, in the middle of the string), all others are erased to have V\textsubscript{T}~3.3V to represent the V\textsubscript{T} majority within an erased V\textsubscript{T} distribution. The V\textsubscript{BL} is then measured with a variety of V\textsubscript{REV} of WL6 as shown in Fig. 8(b), which reveals that at V\textsubscript{REV}=0V and 0.8V as V\textsubscript{BL} flipping voltage, 1.3V offset can be guaranteed. These results are then verified on a test-chip. Although erase distribution under real situation is not available, the reverse verification function can still be exercised intentionally by raised EV voltage up above ground. The offset of sectors is collected and its occurrence probability is plotted in Fig. 9. The mean value is located at about 1.4V which is consistence with the result from the test structure.

Conclusions

A charge-based capacitance measurement technique is proposed to quantitatively validate reverse read function of erase-verify (EV) operation in NAND technology. The internal bit-line voltage during EV can be detected by charge-based capacitance measurement (CBCM) technique. 1.4V shift between V\textsubscript{REV} (reverse read WL bias) and cells’ real V\textsubscript{T} is extracted according to our study. This test structure is easily to be integrated into the advanced technology and we will continuously focus on its application.

Reference

the bit-line capacitor, C

judge whether cell V

In reverse-read sensing, the reverse-read bias voltage

Fig. 2(a) Schematic structure of a NAND array. The

are the levels for program-verify, erase-verify, and

read individually.

Fig. 2(a) Schematic structure of a NAND array. The

V

of the selected WL can be measured individually

with forward-read sensing (V

=1V and V

SSL

=0V). (b) In reverse-read sensing, the reverse-read bias voltage

(V

SSL

=1V and V

GSL

=Vcc)

is used to judge whether cell V

s are low enough to charge up

the bit-line capacitor, C

BL

.

Fig. 6 The waveform to extract the V

SSL

transition during reverse reading. At first, the C

SSL

is discharged via turning on the nMOS.

Fig. 7 (a) The nMOS pulse width and (b) the V

REV

effect on V

BL

. Suitable nMOS pulse width of 0.1μs

−1μs and large V

REV

are easy to obtain a stable V

BL

.

Fig. 8 (a) Schematic representation of the offset between

V

REV, V

BL

of WL6. The V

BL

of WL6 is moving and

others are erased to -3.3V as the majority. The flipping

V

BL

is extracted in (b). It shows that 1.4V offset gets

0.8V of V

BL

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Fig. 3 The test structure is composed of

a NAND string, a CMOS inverter for

charging / discharging the V

SSL

, and one

PMOS capacitor of large area for

storing the charges temporarily.

Fig. 4 Waveforms used to calibrate the pMOS

capacitor. The V

SSL

and V

GSL

is biased at 0V to

isolate the influence of NAND string. Thus, the

capacitor is charged by Ip and discharged by In

along with waveform transition.

Fig. 5 (a) The period time (T

period

) and (b) V

DD

effect on the pMOS loading capacitance (C

L

). Long T

period

and large V

DD

can obtain a stable C

L

.

Fig. 9 Occurrence probability when V

REV

is set at

0.8V. In this case, the maximum probability falls

on 1.4V offset, which is consistent to Fig. 8(b).

Table. MOSFETs features used here.

<table>
<thead>
<tr>
<th>MOS</th>
<th>WL [µm]</th>
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<tbody>
<tr>
<td>3.3V PMOS A</td>
<td>50/10</td>
</tr>
<tr>
<td>3.3V PMOS B</td>
<td>1/0.4</td>
</tr>
<tr>
<td>3.3V NMOS</td>
<td>1/0.4</td>
</tr>
</tbody>
</table>

Fig. 1 Schematic representation of program ("0")

and erase ("1") V

T

distributions. PV, EV, and RD

are the levels for program-verify, erase-verify, and

read individually.