Disturb-free 3D vertical FG NAND with Separated-Sidewall Control Gate

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1. Abstract
In this paper, we intensively investigated the disturbance problems of the 3-Dimensional (3-D) vertical Floating Gate (FG) NAND with Separated Sidewall Control Gate (S-SCG). Above all, we successfully demonstrate fully suppressed disturbance problems, such as indirect programming of the unselected cells, hot electron injection of the edge cells and direct influence to the neighboring passing cells, by using the S-SCG with 30nm pillar size.

2. Introduction
A FG type 3-D vertical Stacked-Surrounding Gate Transistor [1] was proposed in 2001 for the bit cost of NAND flash memory. However, the vertical scaling of the FG type 3-D vertical cell stacked NAND is limited by the interference effect with the neighboring cell. In addition, high Source/Drain (S/D) resistance of unselected cell strings is another critical issue, because the diffused S/D junction cannot be acceptable in vertical cell structure.

For the purpose of overcoming these issues, the Sidewall Control Gate (SCG) with the concept of 3-D FG NAND are receiving attention, such as ESCG [2], DC-SF [3], and S-SCG [4]. Figure 1 shows (a) bird’s-eye view and (b) component of coupling capacitances of the recent 3-D vertical FG NAND with Separated-SCG [4]. By using this structure, High CG coupling ratio with fully suppressed interference characteristics and electrically controlled S/D scheme have been successfully realized. However, the disturbance issues have not been confirmed sufficiently. In this paper, we intensively investigated the disturbance problems of the 3-D vertical FG NAND with S-SCG.

3. Results and Discussion
In order to evaluate the disturbance characteristics of the 3-D vertical FG type cell, we perform 3-D cylindrical device simulations in the vertical direction as shown in Fig. 2 (a). The conventional FG structure without SCG is simulated for comparing to the SCG structure as shown in Fig. 2 (b). Figure 3 shows all of the disturbance problems of recent 3-D vertical NAND with SCG; such as indirect programming of the unselected cells (I), hot electron injection of the edge cells (II) and direct influence to the neighboring passing cells (III). The simulation conditions of theses disturbance problems are also shown in Fig. 3(b).

Figure 4 (a) shows channel boosting potential contours of the program inhibit operation with pillar sizes. As we decrease the pillar size, the surface channel potentials are significantly increased, as shown in Fig. 4 (b) and (c), due to decrease of depletion width. As a result, if we decrease the pillar size below 30nm, the disturbance at the 20V program inhibit operation is fully suppressed due to sufficient channel boosting level as shown in Fig. 5. In addition, Figure 6 shows the channel boosting potentials with SCG, and the SCG voltage suppresses the channel boosting level. However, programming operation occurs in proportion to the potential difference between FG and channel as shown in Fig. 7 (a) and (b). Therefore, as we decrease the pillar size to the 30nm regime, the conventional program disturbance does not occur in 3-D vertical NAND, because the potential difference is within 2V, as shown in Fig. 7 (c).

Sequentially, we verified the indirect programming disturbance issue of edge Word Line (WL) cells, which was mainly caused by hot electron injection in high electric field (E-field) [5]. In Fig. 8, we confirm the E-field contours with the SCG structures. In the SCG structure, the SCG bias (Vscg) mainly determines the E-fields of edge cells, and the program voltage and the space length do not affect the E-field as shown in Fig. 8 (a). In addition, using the 36nm space length, the position of the maximum E-field (Emax) is also 5nm far from FG edge and the area of high E-field over 2MV/cm is also decreased by about 50% by applying a medium bias to the S-SCG as shown in Fig. 8 (b). As a result, the Emax with SCG in the 20V program inhibit operation is lower than that of the conventional FG without SCG, and this Emax can also be controlled by SCG bias as shown in Fig 9 (a). Moreover, as we increase the SCG length, the position of Emax is significantly separated from the FG edge as shown in Fig. 9 (b).

Finally, we confirm the direct influence to the neighboring passing cells. In recent 3-D vertical FG NAND with SCG, the direct disturbance of neighboring passing cells becomes more serious due to the high coupling ratio with the SCG as shown in Fig. 1 (b). In the case of the S-SCG cell, we can combine the Vpass and Vscg to prevent direct disturbance problems as shown in Fig.10 (a) and (b).

4. Conclusions
We intensively investigated the disturbance problems of the 3-D vertical FG type NAND with S-SCG. By using 30nm pillar size, we successfully demonstrate fully suppressing the disturbance in the 20V program inhibit operation of the unselected cells. Moreover, the hot electron injection of the edge cells and the direct influences to passing cells can also be suppressed by controlling the S-SCG bias level.

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References

Fig. 1  (a) Bird’s-eye view and (b) component of coupling capacitances of recent 3-D vertical FG NAND with S-SCG

Fig. 2  (a) The concept of the cylindrical coordination and (b) unit cell structures of the 3-D cylindrical device simulation.

Fig. 3  (a) The disturbance problems of recent 3-D vertical NAND and (b) simulation conditions

Fig. 4  (a) Potential contours and boosting potential distribution of (b) x direction and (c) y direction with pillar sizes

Fig. 5  (a) The boosting potential level of FG and channel and (b) disturbance ΔVth characteristics with pillar sizes

Fig. 6  (a) Potential contours and (b) channel boosting potential distribution of program inhibit operation with SCG structure

Fig. 7  The program Vth with (a) Vcg and (b) ΔV(FG-channel) and potential distributions with Vprog (=Vcg) in program or program inhibit operation

Fig. 8  (a) The E-field contour with program voltage (Vpgm) and spacer length (Lsp) and (b) Potential and E-field distributions at surface channel with SCG structure

Fig. 9  (a) Maximum E-field (E_max) with Program Voltage (Vprog) and (b) Distance of E_max position from FG in edge WL cell with space length

Fig. 10  (a) The direct disturbance ΔVth of the neighboring passing cells and (b) disturbance free window of S-SCG cell with Vscg and Vpass