Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp987-988

A Novel Operating Scheme for 2-bit/Cell Split Gate SONOS Flash Memory

C. H. Chou[1], Steve S. Chung[1], C. -H. Lee[2], T. -M. Hsieh[2], J. -C. Liou[2], C.-H. Chen[3], Patrick ZP Chen[3], and H-H Chen[3]

[1]*Department of Electronics Engineering, National Chiao Tung University, Taiwan*
[2]*Solid State System, Hsinchu Science-Based Industrial Park,Taiwan* [3]*United Microelectronics Corporation (UMC), Taiwan*

Abstract- A novel operating scheme has been proposed for 2-bit/cell split gate SONOS. For a certain design of split gate structure, source-side Injection (SSI) is usually used for programming and band-to-band hot hole injection (BTBHHI) is used for erase. In this paper, programming achieved by forward-bias assisted electron injection(FBEI), erase method achieved by suitable forward-bias assisted hole injection (FBHHI) were proposed. A lower voltage operation and high speed operation has been achieved. These schemes are mainly useful for the 2-bit operation with good electron/hole mismatch and better endurance, data retention, comparing to conventional operation scheme, e.g., SSI or BTBHHI etc.

1. Introduction

In charge-trapping devices, such as SONOS memory, 2-bit per cell operation is the basic requirement of flash memory. For the split gate cell structure [1], in most cases the cell is programmed by channel hot electron (CHE) or source-side injection (SSI), while erase is achieved by band-to-band hot hole injection (BTBHHI). Based on a forward-bias assisted electron injection (FBEI) scheme that we developed in [2], a low voltage, high speed program, and excellent data retention could be achieved. On the other hand, two bits operation has the inherent disadvantages in the mismatch of electrons and holes, which induced the reliability issues [1]. In lieu of the charge pumping technique [3-4], the monitoring of the charge injection as well as the oxide traps can be handled, which facilitate the handling of the mismatch issues.

In this paper, new operation schemes for program/erase, applicable for 2 bit/cell operation in a split gate SONOS cell, has been demonstrated. It is achieved by the so called back-bias assisted electrons and/or holes. The performance can be monitored by a unique CP technique. The verification of the cell performance and the endurance has been demonstrated.

2. Device Preparation

The dual-bit split-gate n channel SONOS with ONO thickness (60/90/90) (A^o), W= 0.2(μm), L_{CG}= 0.18(μm), L_{WG}= 0.13 and 0.10 (μm), as shown in Fig. 1(a) and the n-channel planar SONOS with ONO thickness (50/60/50), W/L= 0.7/0.5(μm), (for comparison purpose), in Fig. 1(b), were fabricated using 0.13 μm technology.

3. Results and Discussion

A. Operation Schemes and Properties of Spilt Gate SONOS

Two modes of pulse operation are shown in Fig. 2, in which (a) shows the unit-pulse mode for conventional operation scheme, e.g., SSI or BTBHHI etc., and (b) shows a multi-cycle pulse mode. A novel operation concept used the multi-cycle pulse series and suitable forward-bias, Fig. 2(b), to enhance the efficiency of program/erase. Based on this idea, Fig. 3(a) is used for the programming, while Fig. 3(b) is used for the erase. In Fig. 3(a), FBEI program, source is floating, during emitting phase T_1, the drain/bulk was forward biased and electrons were injected into the bulk. Subsequently, at T_2, the junction was reverse biased which will cause the previously injected electrons in the bulk to be accelerated across the depletion region and injected into the gate oxide. FBHHI erase is shown in Fig. 3 (b) where substrate is grounded, while gate and drain biases used multi-cycle pulse with variable T_1 and T_2. Erase speed decays, for the pulses in Fig. 3(a), due to the trapping holes at the bottom oxide which leads to a decreasing FN field. The different emitting time T_2 can compensate the degradation of erase speed. The program speed of SSI and FBEI are compared in Fig. 4 , in which the new scheme, FBEI, achieves a faster programming speed. The most noticeable result is that the erase speed was greatly increased when the low voltage of V_D was set at -2V. We understand that the larger V_{high} of drain voltage causes more serious band bending which generates lots of band-to-band tunneling hot hole[5]. In Fig. 6, the drain current was ~3μA in phase T_1, but the current was only ~10 nA even though V_D was swept to 6V. Generally, we can easily create a lot of hot holes by using a slight forward-bias, even if the V_{high} is too low. By using forward-bias on p-n+ junction, we will be able to avoid the junction leakage and breakdown. The result in Fig. 7 exhibits the stable value of leakage current and threshold voltage at V_D= -2V, even up to a thousand seconds .

B. The Monitoring of Stored Charges and Oxide Traps

Figures 8(a) shows the charge-pumping current measurements to identify the trapping charges and oxide traps with the source side floating in a planar SONOS, Fig. 1(b). The curves in I_{CP} plot, Fig. 8(a), shows the existence of injected holes($\Delta I_{CP,h}$), injected electrons ($\Delta I_{CP,e}$), and oxide traps($\Delta I_{CP,Nit}$). The area in the shaded region represents the stored charges. Then, the equations in Table 1 can be used to calculate the charges after the cycling, Eq. (3). The values of $\Delta A/A_0$ can be used as a monitor of electrons, holes, and the oxide traps, which can be used as a monitor of the mismatch between electrons and holes. Table 2 is a combination of different program/erase schemes and the applied biases. Fig. 9(a) show that using FBHHI erase can decrease the rate of oxide degradation and the efficiency of using FBEI/FBHHI combination is much better, comparing to conventional SSI/BTBHHI scheme.

C. Verification of 2 bit/cell operation in Split Gate SONOS

The second-bit effect has also been validated in our split gate SONOS (Fig. 1(a) cell), as shown in Fig.10. Here, from the 45 degree relationship of the new FBEI, it was found that the coupling between the 2 bits was less pronounced in the new FBEI programming scheme. Fig. 11 and Fig. 12 show the endurance characteristics of FBEI/FBHHI (new scheme) and SSI/FBHHI(old scheme). We found that the window closure of SSI/FBHHI is more serious. Furthermore, the comparisons between various operating conditions are listed in Table 3. The multi-cycle pulse schemes kept a superior operation efficiency.

In summary, new operation schemes are demonstrated for a split gate SONOS cell. This new scheme used the same strategy of back-bias assisted electron injection (for program) and hole injection (for erase). Also, it is well suited for two-bit operation. Several salient features of the new scheme include: (1) lower voltage and high speed operation, (2) better mismatch of electrons and holes for 2-bit operation, (3) better endurance as a result of a better control of the charge injections, and (4) expected good retention for reasons of good mismatch.

[1] Y. H. Ho et al., Apl, 97, 183508, 2010.
[2] S. S. Chung et al., in IEDM Tech. Dig., pp. 457-460 , 2007
[3] T. P. Ma et al., in IEEE IEDM, pp. 93-96,1999
[4] H. Pang et al.,in ESSDERC, pp. 209-212, 2005
[5] L. Sun et al.,in JJAP, pp.3179- 3184,2006

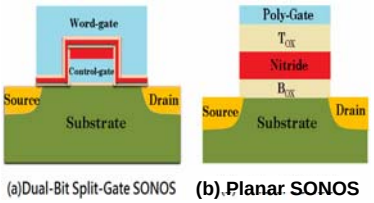

Fig. 1 The schematic structure of the (a) split Gate SONOS and (b) planer SONOS.

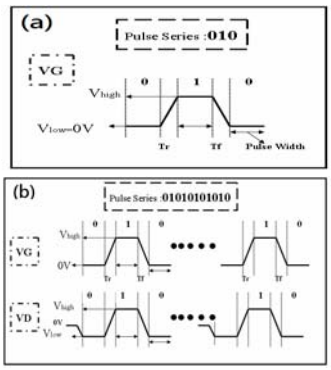

Fig. 2 (a) The conventional unit-cycle pulse series for CHEI or BTBHHI .(b) The multi-cycle pulse series for FBEI or FBHHI in this work.

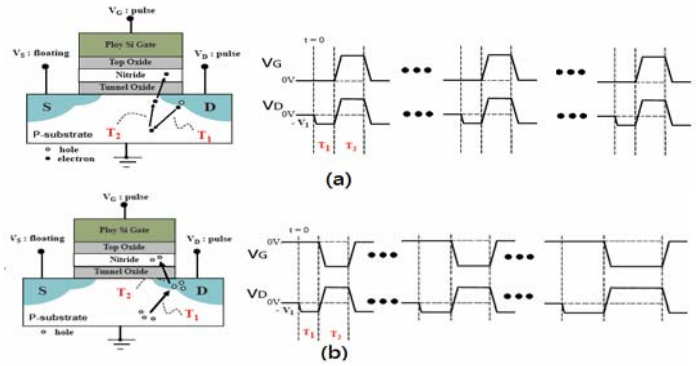

Fig. 3 The operation scheme and timing diagram for (a) FBEI programming and (b) FBHHI erase. The behaviors of electrons and holes in both schemes are different owing to a varying pulse widths for the purpose of controlling electrons/holes injection.

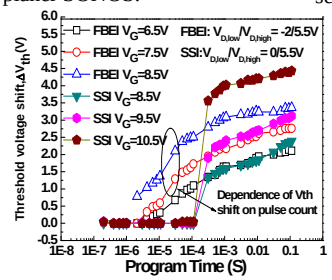

Fig. 4 The comparison of Vth transient between FBEI and SSI. FBEI exhibits a faster transient (i.e., faster speed).

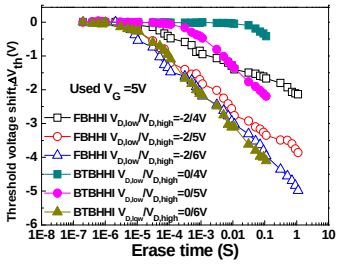

Fig. 5 The erasing transient characteristics with three different voltage conditions for FBHHI and BTBHHI. The erasing efficiency was improved by V_D= -2V.

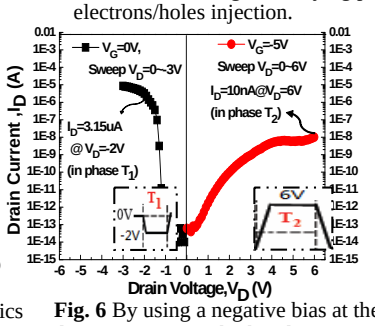

Fig. 6 By using a negative bias at the drain, VD= -2V, a higher drain current current can be obtained. The multi-cycle method improved the erasing efficiency, while it reduces high voltage stress time.

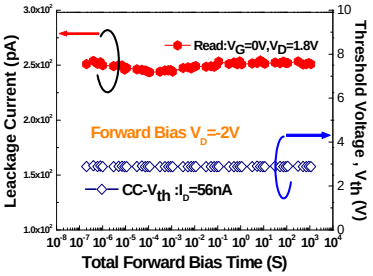

Fig. 7 The leakage current and the Vth shift were not affected by the r accumulated forward bias time.

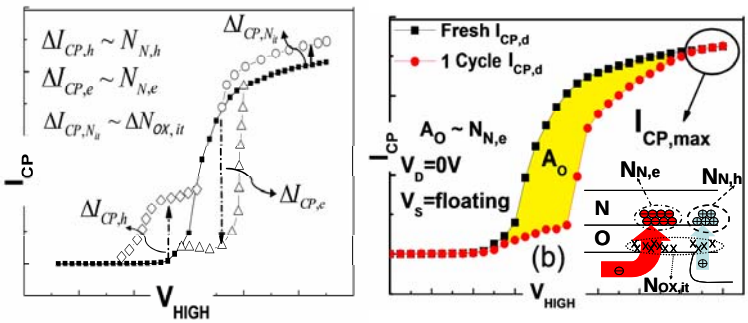

Fig. 8 (a) Charge-pumping current curves related to the trapping charges and interface traps in conventional SONOS. (b) The CP current versus Vh of fresh state (black) and one time programmed state(red).

$$Q_{Pro,total} = \int_0^{L} N_{N,e}(x)dx = \frac{L}{I_{CP,MAX}} \int_0^{I_{CP,MAX}} N_{N,e}(I_{CP})dI_{CP} \quad \text{and} \quad (1)$$

$$= \frac{L}{I_{CP,MAX}} \int_0^{I_{CP,MAX}} \frac{C_{OX}C_N\Delta V_h(I_{CP})}{(C_{OX}+C_N)q}dI_{CP} = \frac{L}{I_{CP,MAX}} \int_0^{Vh(I_{CP,MAX})} \frac{C_{OX}C_N}{(C_{OX}+C_N)q}\Delta I_{CP}(V_h)dV_h$$

1 Cycle $$Q_{Pro@1time} \approx A_o = \int_0^{V_h(I_{CP,MAX})} \left[I_{CP}(fresh) - I_{CP}(1\ \ cycle)\right]dV_h \quad (2)$$

Cycling $$Q_{N,e^-+h^+} \approx A(cycles) = \int_0^{V_h(I_{CP,MAX})} \left[I_{CP}(fresh) - I_{CP}(cycles)\right]dV_h \quad (3)$$

then $$\frac{\Delta A = A(cycles) - A_o}{A_o} \propto N_{N,e} \propto 1/N_{N,h} \propto 1/\Delta N_{OX,it}$$

Table 1 Equations used to calculate the percentage of area A_0 (defined in Fig. 8(b) changes after P/E cycles.

	CHEI	FBEI	BTBHHI	FBHHI
VG	7	7	-6	-6
VD	5	-2/5	5	-2/5
VS	0	floating	floating	floating
Time	1ms	1ms	2ms	1ms
Pulse type	unit-cycle	multi-cycle	unit-cycle	multi-cycle

Table 2 The basic operation conditions of conventional SONOS with various program/erase schemes.

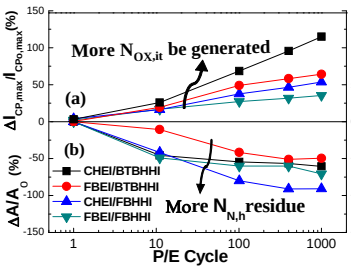

Fig. 9 (a) The $\frac{\Delta A}{A_o}$ and (b) $\frac{\Delta I_{CP,max}}{I_{CPo,max}}$ versus P/E cycle for the four operation conditions.

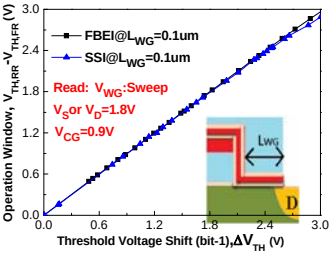

Fig. 10 The window (VRR-VFR) versus Vth shift of bit-1 for split gate SONOS. The second-bit effect can be identified from the 45 degree line.

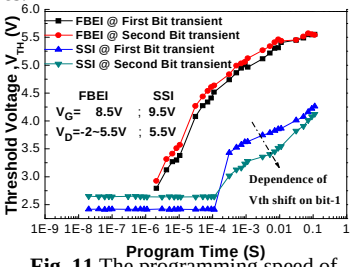

Fig. 11 The programming speed of first bit and second bit by FBEI and SSI. The second-bit transient was degraded using SSI, because the electrons of bit-1 increased the potential peak along the channel.

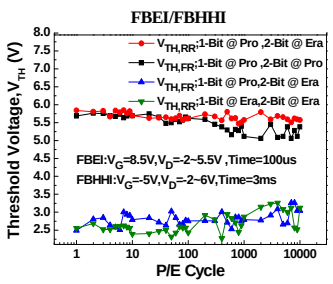

Fig. 11 Endurance characteristics of two-bit-cell application, using FBEI programming and FBHHI erasing (new).

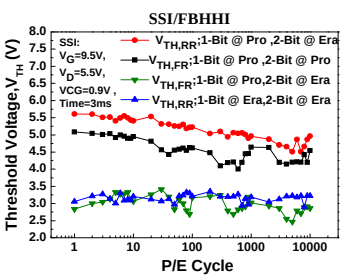

Fig. 12 Endurance characteristics of two-bit-cell application, using SSI programming and FBHHI erasing (old).

	FBEI/FBHHI	BTBHHI	SSI/CHEI
Pulse type	**Multi-cycle**	**Unit-cycle**	**Unit-cycle**
Mode	**One side bias (Vd or Vs)**	**One side bias (Vd or Vs)**	**Two side bias (Vd and Vs)**
Stress time (at pulse V_h)	**Shorter (=0.5*operation time)**	**Longer (=operation time)**	**Medium (=operation time)**
Reliability	1. Low voltage 2. Shorter stress time 3. 2-bit operation is independent.	1. Low efficiency 2. Long erase time	1.High field to generate hot carriers . 2. 2-bit operation is coupled

Table 3 Comparison among three different operation conditions.