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Flexible One Diode-One Resistor Crossbar Resistive-Switching Memory

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Introduction

Flexible electronics have received increasing attention because of the merits of low cost, light weight, and flexibility. However, traditional Si-based memory devices requiring high process temperature are incompatible with flexible substrates with low glass transition temperature. Recently, we have successfully demonstrated both resistive-switching (RS) memories and rectifying oxide diodes fabricated at room-temperature with excellent characteristics [1, 2]. The rectifying oxide diode is applicable to compact one diode-one resistor (1D1R) crossbar architecture to suppress read interference in high-density array through sneaky paths of neighboring cells [3]. In comparison with conventional one transistor-one resistor (1T1R) architecture, $4F^2$ 1D1R not only significantly reduces the cell size, but also enables easy implementation on the low-temperature, low-cost flexible memory array where high-temperature and complicated transistor processes are unfavorable. In this work, we report for the first time a 1D1R memory cell, by a Ni/HfO_2/Pt unipolar RS memory and a Ti/TiO_2/Pt oxide diode, fabricated on a flexible polyimide (PI) substrate. Excellent memory and rectification characteristics are capable of realizing a crossbar 1D1R memory array exceeding 8 kbit with at least 10% readout margin. Furthermore, because all processes were completed at room temperature, the proposed 1D1R cell is promising for flexible, high-density memory applications by roll-to-roll processing at very low cost in the future.

Experiments

A tri-layer of Pt/Ti/SiO_2 was deposited as bottom electrodes on blanket flexible PI films (75 μm thick). To fabricate the Ti/TiO_2/Pt oxide diode, 40 nm TiO_2 was deposited by electron beam evaporation and Ti top electrodes were patterned by shadow-mask technique. To fabricate the Ni/HfO_2/Pt oxide diode, 80 nm HfO_2 was deposited by reactive DC magnetron sputtering and Ni top electrodes were patterned also by shadow-mask technique. All processes were completed at room temperature without additional thermal treatment. The 1D1R cell was characterized by connecting the diode and memory element externally as shown in the schematic of Fig. 1. Figure 2 and Fig. 3 display fabricated flexible RS elements on a PI substrate and the electrical measurement setup for bending conditions.

Results and Discussion

The Ni/HfO_2/Pt memory cell exhibits typically unipolar RS with positive SET/RESET voltages and a resistance ratio of high resistance state (HRS) to low resistance state (LRS) of about 10^3 as shown in Fig. 4(a). The unipolar RS was attributed to the formation of Ni filaments through HfO_2 by Ni ion migration from the top electrode [4]. Rupture and connection of Ni filaments can be performed both at positive polarity by Joule heating and ion migration. Figure 4(b) shows typically unipolar RS of the Ni/HfO_2/Pt memory cell under a severe bending condition with a bending radius of 10 mm. Though the resistance ratio was reduced to 10, largely due to the increase of the HRS current, unipolar RS remained very stable. Figure 5 shows the cumulative distributions of HRS/LRS resistance under various bending conditions. The HRS degradation is still under investigation, but possibly induced by bending strain and bulk defect generation in HfO_2. Fig. 6 shows excellent immunity to read disturb up to 10^3 s for both HRS and LRS.

In Fig. 7, the Ti/TiO_2/Pt oxide diode exhibits excellent rectifying characteristics, including large on/off current ratio (I_{ON}/I_{OFF}= 10^5 at ±1 V), breakdown voltage over ±2 V, and robust endurance up to hundreds of successive DC sweeps. The current rectification was attributed to the asymmetric Schottky barriers at the Ti/TiO_2 and TiO_2/Pt interfaces [1]. The degradation on diode characteristics under bending was negligible. In Fig. 8, by connecting the RS memory and the diode in series, reproducible unipolar RS with substantial R_{HRS}/R_{LRS} ratio were realized at positive bias, while the current at negative bias remained very low due to the reverse-biased diode in series even when the RS memory was at LRS. This helped to suppress the degradation of readout margin due to the sneaky current through unselected bits in a crossbar memory array as shown in Fig. 9. For a worse-case scenario, all unselected bits were at LRS. A simple equivalent circuit in Fig. 10 can be applied to estimate the readout margin for 1D1R crossbar arrays [5]. The sneaky current was determined by $R_R/(M-1)(N-1)$, where R_R was the resistance of the 1D1R cell at reverse-bias. For a 10% readout margin, Fig. 11 shows that the maximum allowed word lines in a square crossbar array increased dramatically from 2 in a 1R array to 92, equivalent to about 8 kbit, in a 1D1R array utilizing the parameters extracted from Fig. 8. The 1D1R array can be further scaled up to 2^{10}x2^{10} or 1 Mbit with an improved R_{LRS}/R_R ratio of $5x10^{-7}$.

Conclusion

A stable Ni/HfO_2/Pt unipolar RS memory and a highly rectifying Ti/TiO_2/Pt oxide diode have been fabricated on a flexible PI substrate using only room-temperature processes. Promising memory and rectification characteristics have been demonstrated even at bending conditions. The series 1D1R cell can effectively suppress the sneaky current and shows promise of realizing high-density flexible crossbar memory at very low cost.

References

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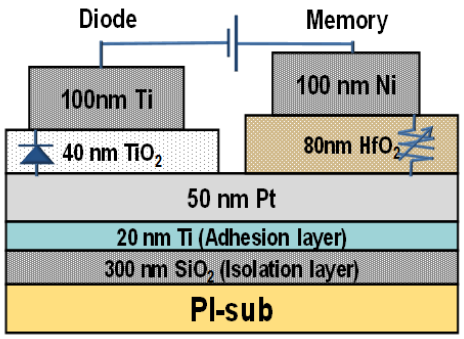


Fig. 1 Schematic of a 1D1R cell by connecting an oxide diode of Ti/40nmTiO_2/Pt, and a RS memory device of Ni/80nmHfO_2/Pt in series.

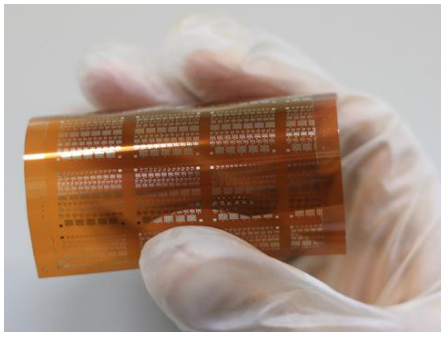


Fig. 2 Photograph of fabricated flexible RS memory devices on a PI substrate.

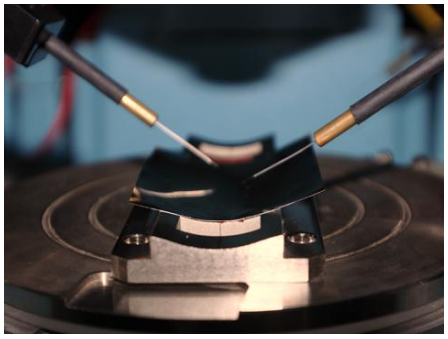


Fig. 3 Photograph of electrical measurement setup and fabricated flexible RS memory devices under bending conditions.

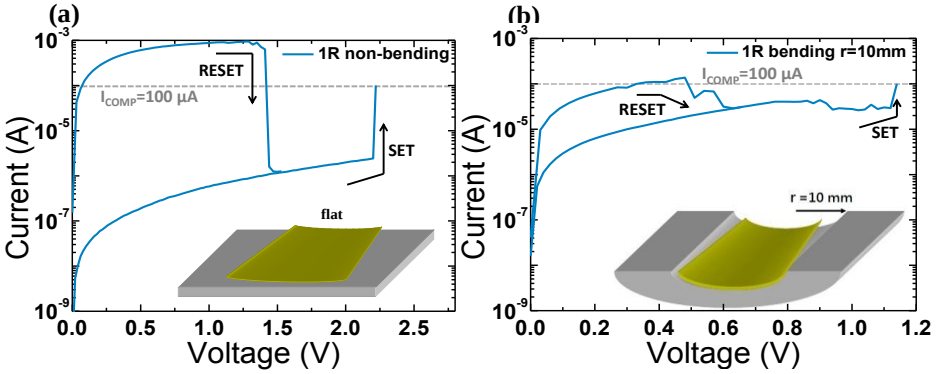


Fig. 4 Unipolar RS characteristics of the Ni/80nmHfO_2/Pt device at (a) flat, (b) bending (r=10 mm) conditions.

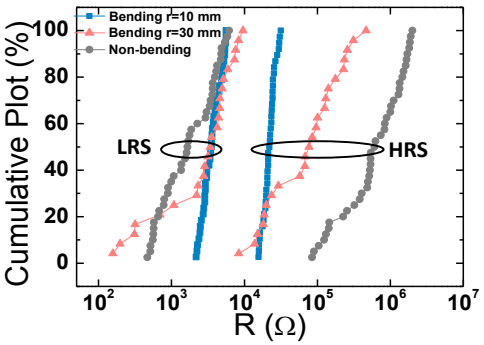


Fig. 5 Cumulative percentages of LRS and HRS resistance of the Ni/80nmHfO_2/Pt device with various bending curvatures.

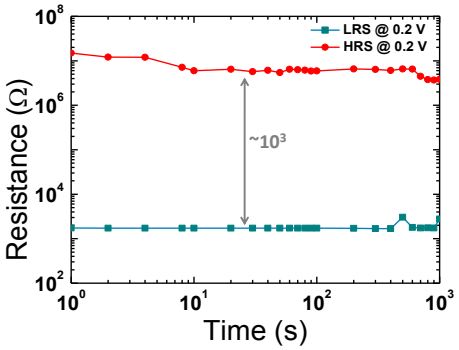


Fig. 6 Read disturbance for HRS and LRS of the Ni/80nmHfO_2/Pt device under constant stress (read) voltage of 0.2V.

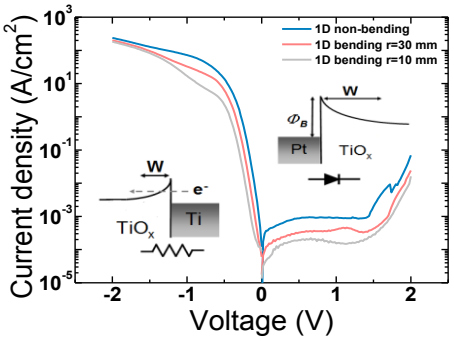


Fig. 7 Rectifying characteristics of the Ti/40nmTiO_2/Pt oxide diode with various bending curvatures.

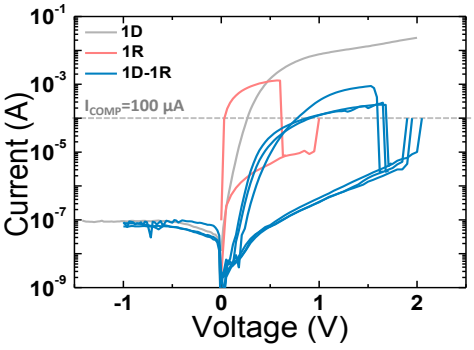


Fig. 8 I-V characteristics of 1D, 1R and 1D1R in series.

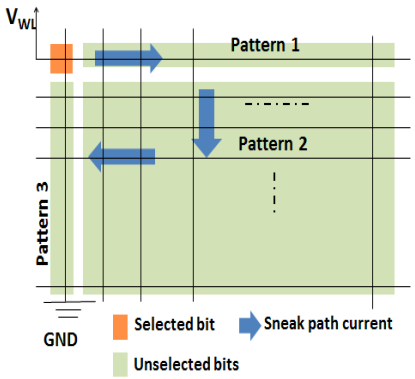


Fig. 9 Schematic showing sneak paths through unselected bits at LRS during read in a crossbar memory array.

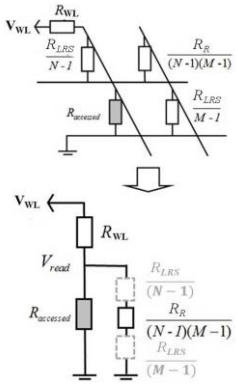
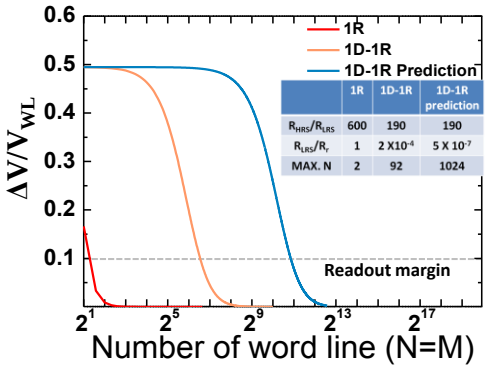


Fig. 10 A simple equivalent circuit used to predict readout margin in a 1D1R crossbar memory array.



	1R	1D-1R	1D-1R prediction
R_{HRS}/R_{LRS}	600	190	190
R_{LRS}/R_r	1	2×10^{-4}	5×10^{-7}
MAX. N	2	92	1024

Fig. 11 Calculated readout margin as a function of the number of word line in square (N=M) crossbar 1R and 1D1R arrays.