Effects of Ti interfacial layer on resistive switching memory performance using Cu filament in high-κ Ta₂O₅ solid-electrolyte

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1. Introduction

Recently, many resistive random access memory (ReRAM) devices using binary oxides such as NiO, Ta₂O₅, ZrO₂, Gd₂O₃, HfO₂, TiO₂, etc have been reported for future nanoscale nonvolatile memory applications. However, the resistive switching mechanism of ReRAM devices is not understood clearly. On the other hand, conductive-bridge ReRAM devices with different solid-electrolytes such as GeSe, GeS, Ti₅O₆, ZrO₂, SiO₂, [1-8] etc have been also reported by several groups. In this case, the silver (Ag) or copper (Cu) can be used as electrodes of the mobile ions. Under an external bias on Ag or Cu electrode, the metallic filament can be formed (or dissolved) in to the solid-electrolyte films. It is realized that the Cu (or Ag) ions diffusion is difficult to control through a single layer of solid-electrolyte. So Ti interfacial layer between the Cu top electrode and Ta₂O₅ solid-electrode will not only improve the resistive switching performance but also will improve the adhesion. In this study, the improved resistive switching memory performance using Ti interfacial layer in an Al/Cu/Ti/Ta₂O₅/W structure has been investigated for the first time.

2. Experiment

A tungsten (W) metal as a bottom electrode was deposited by sputtering on SiO₂/Si substrate. The thickness of W is approximately 100 nm. After that the SiO₂ layer with a thickness of 150 nm was deposited on the W/SiO₂/Si substrate. Different device areas from 150x150 nm² to 8x8 μm² were fabricated by using lithography and etching process. Finally, the lift-off process was used to fabricate this resistive memory device. The high-κ Ta₂O₅ solid-electrolyte with a thickness of 15 nm was deposited by E-gun evaporator using pure Ta₂O₅ shots. Then, a thin Ti layer with a thickness of ~ 2 nm was deposited by E-gun using Ti shots. Ti layer can be used as a good adhesion between Cu and Ta₂O₅ films. The effective barrier height at the Ta₂O₅/Cu interface could be reduced due to Ti interfacial layer. After deposition of Ti layer, oxygen can be gathered in that layer which can be a TiO₂ layer. This oxygen will come from Ta₂O₅ solid-electrolyte. Finally, bi-layer TiO₂/Ta₂O₅ solid-electrolyte could be obtained. The TiO₂ layer will control the diffusion of Cu ions under external positive voltage on the top electrode. The Cu as a mobile metal layer with a thickness of 50 nm was deposited by thermal evaporator. Then, Al as a top electrode with a thickness of 160 nm was deposited in-situ by the same thermal evaporator. The device was annealed at 350°C in N₂ ambient for 1 min. Fig. 1 shows the schematic view of our novel resistive memory device with Ti interfacial layer. More than twenty resistive memory devices were measured to realize the device performance.

3. Results and discussion

Fig. 2(a) shows good conformal deposition of Ta₂O₅ solid-electrolyte film on W layer. The thickness of Ta₂O₅ film is approximately 15 nm. The Ta₂O₅ film shows amorphous [Fig. 2(b)]. The W, Ti and high-κ Ta₂O₅ layers are confirmed by EDX analysis [Fig. 3]. The high-κ Ta-rich Ta₂O₅ film is also confirmed by x-ray photoelectron spectroscopy (not shown here). The current-voltage hysteresis (I-V) loop of w/o Ti interfacial layer resistive memory devices with a current compliance (Icc) of 500 μA, and repeatable 100 consecutive DC cycles is shown in Fig. 4. Applied sweeping voltage is shown by arrow 1→4. A large dispersion of low resistance state (LRS) is observed due to uncontrolled Cu ions diffusion as well as electron injection current. A small resistance ratio (HRS/LRS) of <10 is observed for w/o Ti interfacial layer. Excellent repeatable I-V switching is observed for w/ Ti interfacial resistive switching memory device (Fig.5). It is noted that effective barrier height of Ta₂O₅ film could be reduced by introducing Ti interfacial layer. So the electron injection current could be controlled as well as the Cu ion diffusion in to the Ta₂O₅ solid electrolyte. Although the high resistance state (HRS) is varied with cycle-to-cycle as compared to that of w/o Ti interfacial layer, which may be due to the large resistance ratio of >10². The resistance ratio is further increased with increasing the Ti layer thickness from 2-5 nm (not shown here). The SET voltage is varied from 0.22-0.5V (Fig. 6). The HRS is varied from 200k-100MΩ while the LRS variation is negligible from 0.8-1kΩ (Fig. 7). The LRS is almost unchanged with different device area (not shown here). It implies that the Cu filament is formed during external bias. The HRS increases with decreasing the device size due to lower defects as well as lower leakage current. The LRS decreases with increasing Icc (Fig. 8), due to the Cu filament diameter increased (Fig. 8). The crystalline Cu filament is observed under external bias (not shown here). Excellent read endurance of >10⁶ times (Fig. 9) and program/erase endurance of >10⁷ cycles (Fig. 10) are observed owing to the Ti interfacial layer resistive memory device design. Excellent retention characteristics with a large resistance ratio of >10² after extrapolation of 10 years data retention are observed (Fig. 11). The HRS is almost unchanged but the LRS is increased with elapsed time. This may be the scattering of Cu metals from the filament surface or metallic behavior of Cu filament by native TiO₂ and TaO₂ films.

4. Conclusion

Novel resistive memory device with Ti interfacial layer in an Al/Cu/TiO₂/Ta₂O₅/W structure with a large resistance ratio of >10² , excellent endurance of 10⁷ cycles and extra-plotted 10 years data retention is reported. The resistive memory device could be operated as current as 1 μA. This resistive memory device is very useful in future nonvolatile memory devices below 20 nm technology node.

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References

A memory device using Al/Cu/Ti/Ta₂O₅/W structure is shown in Fig. 1. The schematic view of the resistive memory device is depicted using a top and bottom electrode, with SiC and SiO₂ layers.

Fig. 2(a) shows a high-resolution transmission electron microscope (HRTEM) image of the Al/Cu/Ta₂O₅/W resistive memory device structure. The device area is approximately 1.0 μm². (b) Thickness of the Ta₂O₅ film is 15 nm. The Ta₂O₅ film shows amorphous.

Energy dispersive x-ray spectroscopy (EDX) shows W, Ta₂O₅, and Ti layers from Fig. 2(b).

Fig. 3 shows an energy dispersive x-ray spectroscopy (EDX) image with intensity (arb.units) vs energy (keV). This confirms the presence of W, Ta, and Cu layers.

Fig. 4 illustrates a current-voltage (I-V) hysteresis loop of w/o Ti interfacial layer. The LRS shows a large dispersion. A small resistance ratio of <10 is observed.

Fig. 5 displays an I-V hysteresis loop of w/ Ti interfacial layer resistive switching memory device. A negligible LRS dispersion is observed. A large resistance ratio of >10⁴ is also obtained.

Device area: 150×150 nm². The Ti interfacial layer is observed with increasing current compliances owing to Cu filament diameter increased.

Fig. 6 is a Weibull plot of the SET voltages of our bi-layer TiO₂/Ta₂O₅ solid-electrolytes resistive switching memory devices. Cycle-to-cycle and device-to-device characteristics are shown.

Fig. 7 is a Weibull plot of the HRS/LRS with cycle-to-cycle and device-to-device. A large resistance ratio of >10⁴ is observed.

Fig. 8 shows a current compliance (A) vs resistance (Ω) for the LRS state. The average value is indicated.

Fig. 9 illustrates the read endurance of w/ Ti interfacial layer resistive memory device. A large read endurance of 10⁷ times could be measured with a read voltage of +0.2 V. Due to the large read voltage of +0.2 V, it will be easy to design the memory circuit.

Fig. 10 presents program/erase endurance characteristics of w/ Ti interfacial resistive memory devices. An acceptable resistance ratio of >10 is observed. A good endurance of 10⁷ cycles is obtained, due to the Ti interfacial layer.

Fig. 11 shows excellent retention characteristics of the Ti interfacial resistive switching memory devices. The retention ratio is more than 10⁷ after extrapolation of 10 years data retention. This novel resistive switching memory device is very useful for future nanoscale nonvolatile memory applications.