Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1047-1048

Experimental Comparison of Process Variation in 65nm and 180nm CMOS Using Ring Oscillators with Adjustable Delay

T. Ansari, W. Imafuku, M. Yasuda, S. Sasaki, H.J. Mattausch and T. Koide

Research Institute for Nanodevice and Bio Systems, Grad. School of Advanced Sciences of Matter, Hiroshima University.
739-8527, Higashi-Hiroshima, Kagamiyama 1-4-2, Japan.
Phone: +81-082-424-6265. E-mail: ansaritania@hiroshima-u.ac.jp

1. Introduction

The process parameters of a CMOS technology can vary lot-to-lot, wafer-to-wafer, and die-to-die. Even though there have been advancements in lithographic technology to reduce the size of variation of identically-drawn devices, random performance distributions of these devices still occur because of variations in doping densities, oxide thicknesses, and diffusion depths, just to name a few [1-3]. This variation is of critical importance in both analog and digital circuit designs, especially in circuits that rely on relative device matching [2,4]. Here, we report the 2-dimensional variation in a 1.3mm×1.28mm test chip fabricated with 65nm CMOS technology and a comparison to 180nm CMOS technology results. Our data shows that within a die, the 65nm CMOS variation is 4 times larger than that for 180nm CMOS.

2. Structure of test circuit and measurement procedure

The test chip [Fig. 1] consists of 128 ring oscillator occupying 1.3mm × 1.28 mm area and fabricated in 65nm CMOS. Each ring oscillator has 256 delay blocks with an activating NAND gate. The 256 blocks are divided into an upper and a lower part having 128 stages each [Fig. 2]. The layout area of each ring oscillator is 1200um ×10um. In the delay blocks, there are 2 paths. Path 1 has to go through a transmission gate and an inverter and the delay is termed as τ_{1s}. Path 2 is gated and has a delay block where additional delay is created with an inverter chain and its overall delay is termed as τ_{2s}. The choice of any path is selected through a control signal. With the help of a logic analyzer and a frequency meter, the frequency/time periods of a targeted ring oscillator have been collected for different locations of the delay setting τ_{2s}.

3. Measurement results

The delay of a single block τ is the difference between τ_{1s} and $\tau_{2s,}$ ($\tau=\tau_{2s}-\tau_{1s}$) and its variation has been analyzed for location changes in horizontal and vertical directions. The determined τ variation characterizes the within-die variation nature of an identical circuit structure in horizontal direction using data from the 256 blocks of one ring oscillator. The τ variation at fixed horizontal positions in different rows gives the variation trend along the vertical direction. For the reported analysis, rows from top, middle and bottom sections of the die have been chosen.

Table I shows the variation of τ in a die along the horizontal axis with mean (μ) and 1-sigma (σ) for three different dies over a distance of 1.3 mm. Data shows that $3\sigma/\mu$ is 7.19%~6.07% (die1), 6.74%~5% (die 2) and 6.29%~4.68% (die 3), respectively. The 1-σ distribution is purely random in nature and correlation is not observable, which confirms the purely random nature of the variation with no systematic errors. Also, the μ values show that there is no persistent systematic variation in any die. Table I additionally shows the comparison of the τ variation of a single delay block from 3 different dies for 180 nm [4] test chips. The $3\sigma/\mu$ (%) values for a row reveal that the amount of horizontal variation for 65 nm is much larger than for 180 nm CMOS. Even though the distance in horizontal direction is 1.6 times larger in 180 nm case, the measured horizontal variation of τ for 65nm technology proves that $3\sigma/\mu$ (%) is 4~7 times increased over the 180 nm technology. Table I also reveals that the value of $3\sigma/\mu$ for 65 nm at a particular position in die is changing 1.5 times from maximum to minimum value for 3 different dies, while this change is around 2 times for 180nm CMOS. This result (although only for 3 dies) indicates that the main variation increase from 180nm to 65nm CMOS comes from the within-die variation.

For the vertical analysis, we have chosen sixteen position along the upper section of a ring oscillator (example, delay stage 1, 9, …128) in a die. Here, the delay has a slight increase on the right side of the die and this is common for the 3 analyzed dies which may point to a systematic variation in the die [Fig. 3], which may be caused by the power supply layout. Table II listed the measured μ, 1-σ and $3\sigma/\mu$ for 65nm CMOS at different vertical positions for rows and a comparison is done with previous 180nm [4] test data. The apparently larger variation in vertical direction for 180nm CMOS is mainly explained by a systematic variation in vertical direction.

3. Conclusions

Here, we have analyzed location based 2-dimensional process variation in 65nm CMOS and compared our results to that of 180nm CMOS. The measurement data showed 4 times larger within-die variation for 65nm in comparison to 180nm CMOS. Special attention is needed for effective power supply routing because the measurement data may reflects insufficiencies as a systematic variation.

Acknowledgements

The VLSI chip was fabricated through the chip fabrication program of VLSI Design and Education Center

(VDEC), the University of Tokyo, in collaboration with STARC, Fujitsu Co., Cadence Design Systems Inc. and Simucad Design Automation Inc.

References

[1] K. Bernstein, *et al*, *IBM J. of Research and Development*, vol. 50, pp. 433 – 449, July/Sep. 2006.

[2] L.-T. Pang, B. Nikolić, "Measurements and analysis of process variability in 90nm CMOS", IEEE J. of Solid-State Circuits, vol.44, no.5, pp. 1655-1663, May 2009.

[3] Xin Zhang, et.al, pp. 109 – 110 ASP-DAC, 2011

[4]T. Ansari, et al. "Analysis of Within-Die and Die to Die CMOS Process Variation with Reconfigurable Ring Oscillator Arrays" Jpn, J, of Appl. Phys, 50(2011) online.

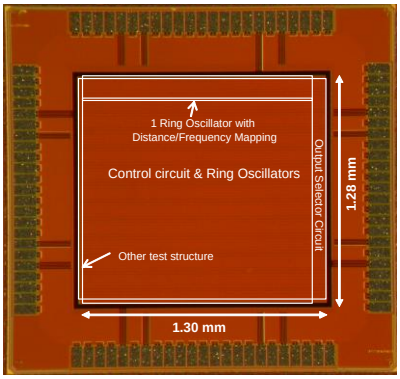

Fig. 1: Micrograph of the test chip

Table I: Measurement data for horizontal analysis

		65nm test data		65nm (1.3 ×1.28 mm^2)	180nm[4] (1.69 ×1.59 mm^2)
		Mean (ps)	Sigma (ps)	3σ/μ (%)	3σ/μ (%)
Top Side	Die 1	271.05	6.500	7.19	1.0
	Die 2	268.64	6.0324	6.74	2.01
	Die 3	264.13	4.1208	4.68	1.63
Middle Side	Die 1	268.60	5.4386	6.07	1.26
	Die 2	277.39	4.6339	5.01	1.96
	Die 3	261.51	4.7382	5.44	1.33
Bottom Side	Die 1	271.85	6.2358	6.88	3.16
	Die 2	268.19	4.7466	5.31	2.34
	Die 3	261.54	5.4821	6.29	1.39

Table II: Measurement data for vertical analysis

	65nm test chip			180nm [4]
Block Position	Mean (ps)	Sigma (ps)	3σ/μ (%)	3σ/μ (%)
113	262.18	7.4545	8.25	10
89	260.44	7.2624	8.37	15
41	262.79	7.6888	8.78	19
1	264.71	7.5134	8.52	20

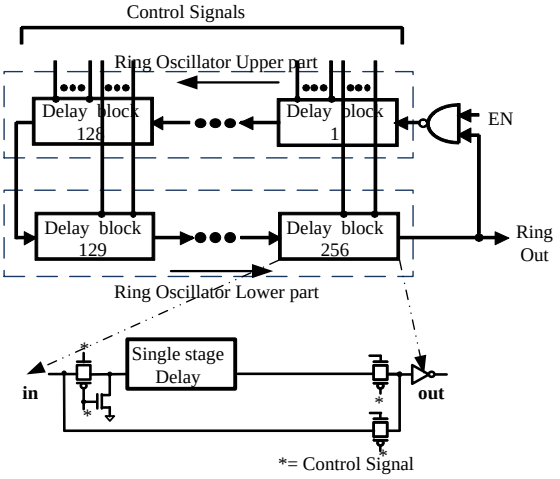

Fig. 2: Basic block diagram of a ring oscillator and detailed schematic of a delay block

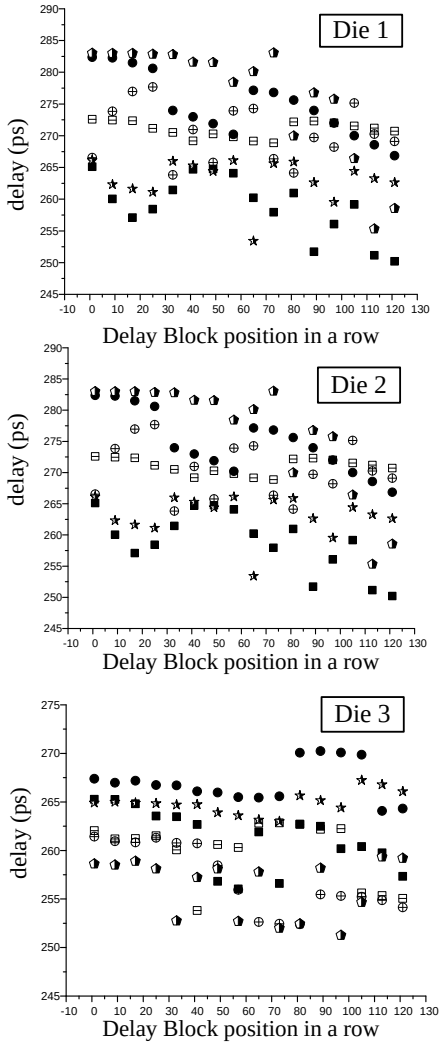

Fig. 3: Delay along different vertical position in a die