

Effect of Resin-Molded Package Structure on Silicon Chip Surface Stress Distribution

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1. Introduction

The rapid expansion of sophisticated mobile devices, such as smartphones, requires the development of smaller and more precise electronic components. In particular, power management integrated circuits (ICs) require higher-accuracy operation to more efficiently use the limited energy supply of a lithium-ion battery. One factor detrimental to IC accuracy is the residual stress resulting from the resin-molded packaging process [1] [2]. However, there is little information available on the effect of packaging-induced stress on small-scale ICs.

This paper presents a characterization of packaging-induced stress distributions on the surface of a small-scale silicon chip representative of power management ICs. Specifically, the effects of both chip size and package structure are discussed.

2. Experimental

In the present study, a piezoresistor embedded in a silicon chip is used as a stress sensor (Figs. 1 and 2). The piezoresistors are small enough to be arranged in a lattice-like pattern, allowing visualization of the stress distribution over an entire chip. Using our calibration system, each piezoresistance coefficient can be determined experimentally under controlled uniaxial loading (Fig. 3).

Because only one piezoresistor can be mounted on each test chip, multiple test chips were fabricated, each with a different piezoresistor position. The resistance shifts between packaging stages were measured by die-to-die correspondence, and the results were reproduced on a single distribution chart (Fig. 4). Biaxial stress components were then calculated using the resistance shifts and the piezoresistance coefficients [3] [4] [5].

3. Results and Discussion

Distribution charts of the x - and y -direction stress components (S_x and S_y , respectively) for a 0.8×1.2 mm test chip are shown in Fig. 5. The compressive stresses are greatest at the center of the chip and gradually decrease toward the edges, with a range of approximately 40 MPa in S_y . Centerline S_y stress distributions of three similarly packaged but differently sized test chips, varying only in y -dimension, are shown in Fig. 6. Both the maximum stress and the stress distribution range decrease by reducing the y -dimension of the chip. Therefore, the selection of a smaller silicon chip is an effective means of minimizing

stress-induced changes in performance.

The effect of package structure on stress distribution was also investigated using the two test chip configurations shown in Fig. 7. Sample A is the same as the chip depicted in Fig. 5. Sample B features a chip tab that is smaller than that of Sample A and is also smaller than the silicon chip. A distribution chart of S_y for Sample B is shown in Fig. 8. Unlike Sample A (Fig. 5), the maximum compressive stress is outside of the central area.

The centerline S_y stress distributions of both samples are compared in Fig. 9, and differ dramatically. The peripheral area of Sample B shows higher stresses (above 100 MPa) than Sample A, whereas the central area of Sample B has similar stress intensity. This central area, which is nearly equal in size to the chip tab area, is suitable for circuit components that require higher-accuracy operation, such as pair transistors and resistor ladder networks widely used in analog circuitry, because the mismatch characteristics can be maintained relatively constant throughout the packaging process. The difference in stress distribution of the two samples is attributed to the variation in chip tab structure.

4. Conclusions

The residual stress in small-scale silicon chips resulting from the resin-molded packaging process was evaluated, which displayed the stress distribution with high resolution. Smaller-sized silicon chips benefit from a narrower stress distribution.

In addition, the study reveals that the chip tab structure has a direct effect on stress distribution. Although a small chip tab generates a constant stress at the central area of the silicon chip, the peripheral area shows higher stresses (above 100 MPa for the sample evaluated). Therefore, a chip tab should be carefully sized to improve the accuracy of small-scale analog ICs.

References

- [1] N. Ueda et al, Int. Conf. on Micro. Test Struct., ICMTS, 2008.
- [2] N. Ueda et al, IEEE Trans. on Semi. Manuf., Feb vol.22, 2009.
- [3] N. Ueda et al, Int. Conf. on Solid State Devices and Materials SSDM 2009.
- [4] N. Ueda et al, Int. Meeting for Future of Electron Devices, Kansai, IMFEDK, 2010
- [5] N. Ueda et al, Int. Conf. on Solid State Devices and Materials SSDM 2010.

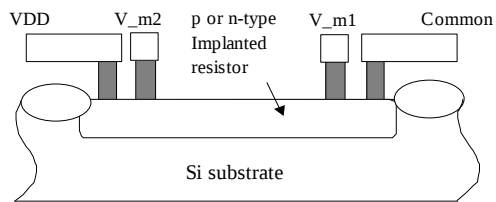


Fig. 1 Cross-sectional chart of the piezoresistor.

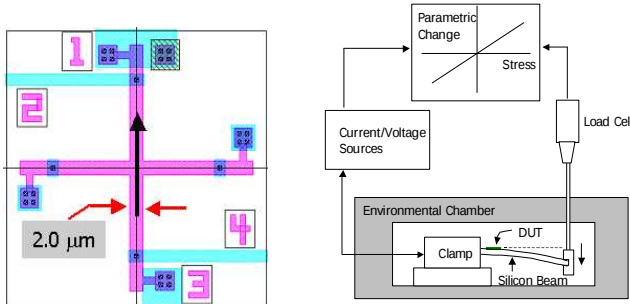


Fig. 2 Plane view of the piezoresistor. Fig. 3 Calibration system.

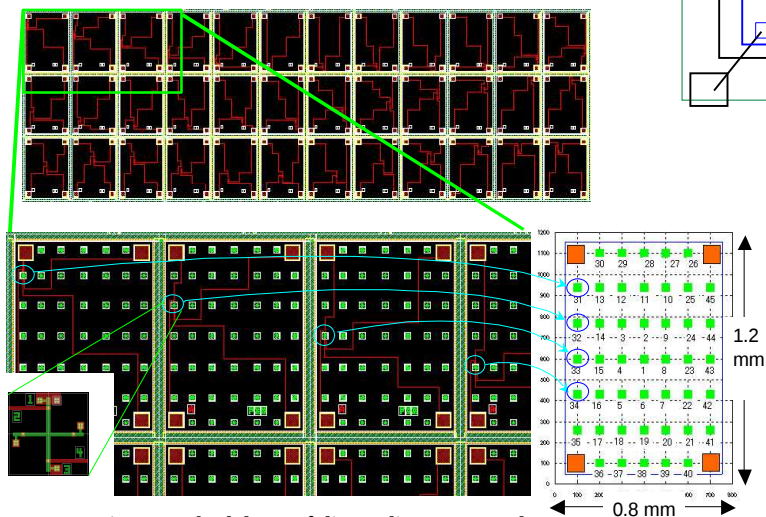


Fig. 4 Methodology of die-to-die correspondence.

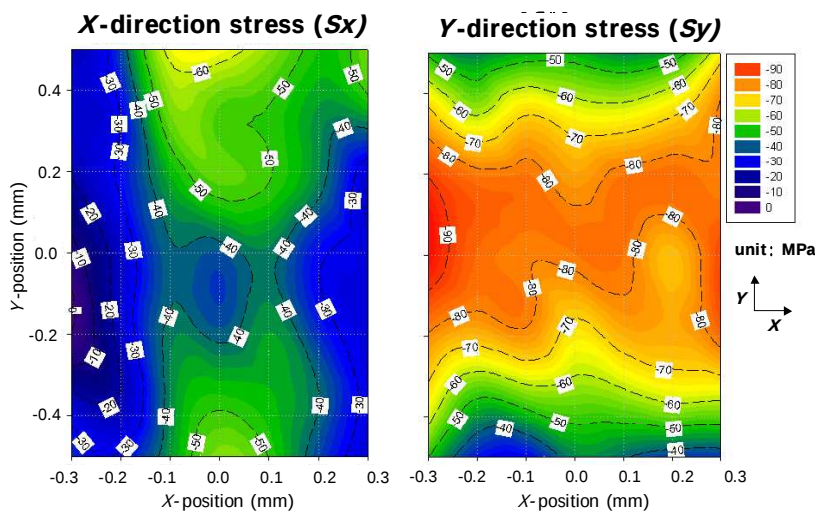


Fig. 5 X- and y-direction stress distributions for a 0.8 mm × 1.2 mm silicon chip.

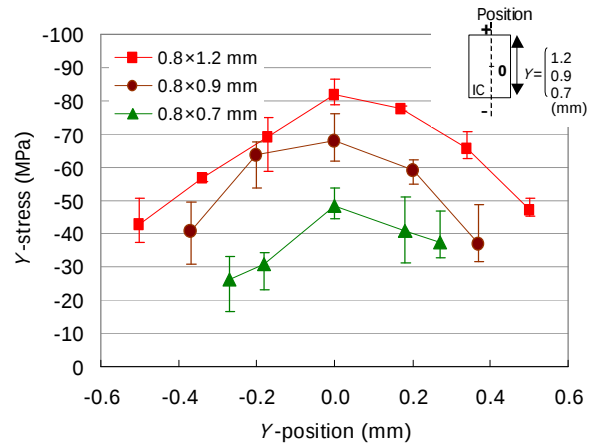


Fig. 6 Centerline y-stress distributions for three chip sizes.

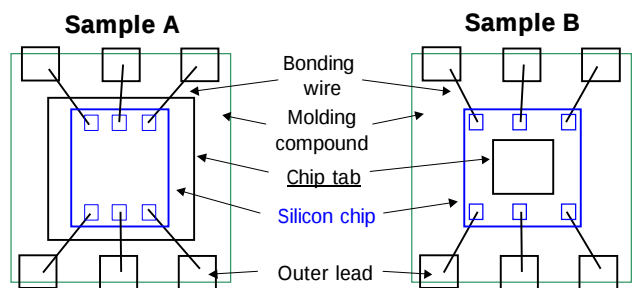


Fig. 7 Outline drawings of two test chip configurations.

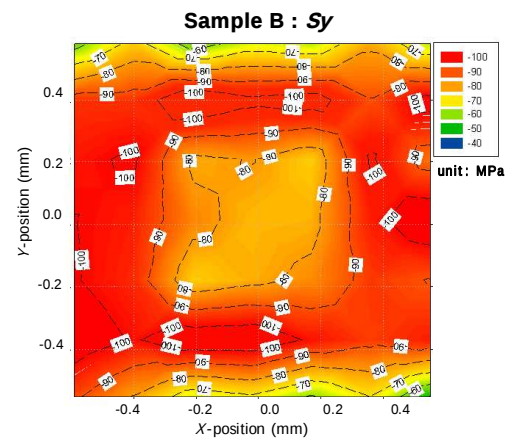


Fig. 8 Y-stress distribution for Sample B.

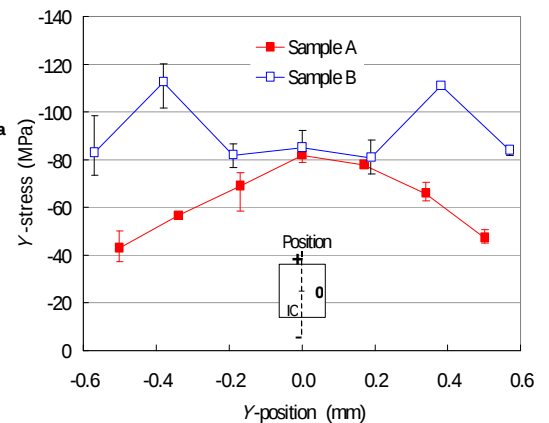


Fig. 9 Centerline y-stress distributions for Samples A and B.