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Challenges and Trends of Resistive Memory (Memristor) Based Circuits for 3D-IC Applications

Meng-Fan Chang[1], Pi-Feng Chiu[2], Ching-Hao Chuang[1], Che-Wei Wu[1], Mon-Shu Ho[3], Ping-Cheng Chen[4], Shyh-Shyuan Sheu[2], Ming-Jinn Tsai[2], and Tzu-Kun Ku[2]

[1] National Tsing Hua University
EECS Bldg., 101, Sec. 2, Kuang-Fu Road,
Hsinchu 30013, Taiwan
Phone: +886-3-516-2181 E-mail: mfchang@ee.nthu.edu.tw
[2] EOL, ITRI, Hsinchu, Taiwan
[3] National Chung Hsing University, Taichung, Taiwan
[4] I-Shou University, Kaohsiung, Taiwan

1. Introduction

Three-dimensional die-stacking (3D-IC) technologies not only achieve heterogeneous integration with a small form factor, but also improve the speed and power performance of a system, as compared to multiple-chips-on-a-PCB designs. A through-silicon-via (TSV) is a promising 3D die-stacking solution because of its higher density, smaller interconnect RC, potential for realizing a larger bandwidth using wide-IO, and has less limitations on the maximal number of stacked layers (N_{STACK}) [1-3], as compared to previous wire bonding and vertical circuit interconnect technologies. However, the TSV-based 3D structure does not achieve significant power and peak-current reduction ratios over the 2D designs [3]. This causes concern about the thermal and power integrity crises of 3D-ICs.

Fig. 1 compares the performance of volatile, nonvolatile (NVM), and emerging nonvolatile memories (ENVMs). The most commonly used NVMs are flash memory [4]-[6]. Due to speed and VDDmin gaps between SRAM/DRAM and NVMs, many mobile chips use SRAM/DRAM for fast/low-VDDmin access and flash for data-backup instead of a single eNVM macro. Smart use of the power-off mode can reduce the system standby current. However, the word-by-word (serial) data transferring between the volatile and non-volatile memories during power on/off operations consumes significant power and long access delay. Moreover, the large peak current consumed by flash memory causes significant power integrity degradation for 3D-IC, especially with a large number of stacked layers.

Several emerging nonvolatile memories (ENVMs), including phase-change RAM (PRAM) [7]-[11], magnetic RAM (MRAM) [12]-[15], conductive-bridge RAM (CBRAM) [16], [17], and resistive RAM (RRAM), have been proposed. These emerging memories are nonvolatile, while supporting faster operating speeds and lower dynamic power than those of conventional flash devices. Resistive memory (RRAM/memristor) [18]-[31] is one of the most promising ENVMs because of faster write time, large R-ratio, multilevel capability, and relatively small write power consumption.

This paper discusses circuit design challenges and trends in using RRAM macros and memristor-based non-volatile logics and SRAMs to achieve faster system speed and reliable system operation, while demonstrating lower power consumption in relieving thermal effects for 3D-ICs.

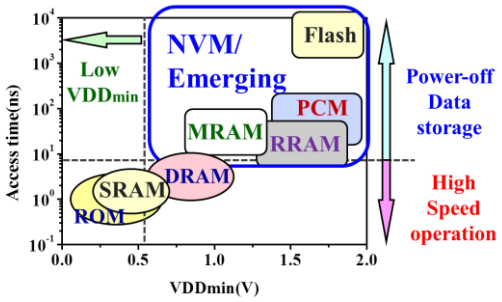


Fig. 1. Speed vs. VDDmin for various memories.

2. RRAM Macros in 3D-ICs

Fig. 2(a) shows the conventional memory architecture for 3D-ICs using SRAM, DRAM, and NVMs. The data in SRAM/DRAM is stored to NVM during power-off operations and restored to the DRAM/SRAM during power-on operations. These store/restore operations consume significant time and power, especially using the flash memory.

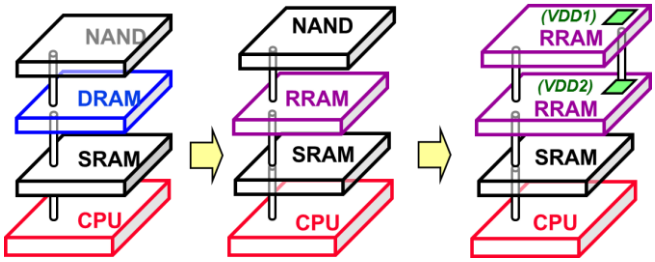
Thanks to the fast random read write speed, both RRAM and MRAM enable the alternative memory architecture for 3D-ICs without using DRAM, as Fig. 2(b) shows. Using this SRAM-ENVM structure, the 3D-IC can achieve lower power consumption by eliminating the DRAM self-refresh power and power consumption due to DRAM-NVM data transfer. Magnetic RAM has a high write speed and excellent endurance, but suffers from challenges in sensing yield due to a limited R-ratio. Considering the poor power integrity in 3D-IC [3], MRAM suffers significant sensing challenges across various PVT conditions in a larger N_{STACK} 3D-IC system.

RRAM currently exhibits drawbacks in limited endurance and wide resistance distribution. Thanks to its larger R-ratio, RRAM has potential to achieve more reliable read operation than can other ENVMs for 3D-ICs with larger N_{STACK} against power integrity degradation if wide re-

sistance distribution challenges can be overcome. Because of lower write current and more reliable read operation, RRAM is more suitable as the main NVM storage in a 3D-IC system, as compared to using flash or other ENVMs for the normally read application (with less endurance constraint).

A novel sensing scheme was proposed to achieve sub-8ns random access time with high sensing yield against wide resistance distribution for a 4Mb RRAM macro [31]. This sensing scheme not only enables the RRAM macro to achieve faster read speed, but also facilitates reliable read operation against power integrity degradation in a larger N_{STACK} 3D-IC system.

To reduce power consumption further and improve power integrity, the 3D-IC can additionally apply multiple supply voltages (VDD) dynamically to various RRAM layers according to the PVT condition of each layer, thanks to the reliable sensing behavior of RRAM, as Fig. 2(c) shows.



(a) (b) (c)

Fig. 2. (a) Conventional; (b) RRAM-based memory architectures; and (c) multiple-VDD schemes for 3D-ICs.

3. Memristor-based Nonvolatile Logic and SRAM in 3D-ICs

Low power operation, thermal stress and reliable data back-up against sudden power failure are critical challenges for battery-powered 3D-ICs. Unfortunately, for nanometer chips, large standby currents consume significant power and thermal stress. Applying power-off mode may reduce the standby current for 3D-ICs if the data backup does not consume significant power. However, the temporary computation status or states would be lost if the power supply is down due to sudden power failure or energy-saving power-off mode. Therefore, preserving the temporary status of each sub-block during power-off operation is necessary.

Using nonvolatile logics [23], [32], such as nonvolatile latch and flip-flops, numerous sub-blocks can be shut-down to reduce standby power without status loss, lengthening the battery life time and relieving the thermal stress for 3D-ICs. Fig. 3 shows the structure of the proposed memristor-based latch and flip-flops.

Researchers have proposed several nonvolatile-SRAMs (nvSRAMs) to provide a more favorable solution for mobile chips, thanks to their fast bit-to-bit parallel data storage. These works include SONOS-12T cell [33], MRAM-19T2R latch [34], Fe-capacitor-6T2C cell [35], PCM-7T2R [36] cell, RRAM-6T2R cell [37], and our proposed RRAM-8T2R cell [38]. This 8T2R cell achieves low-power and high-speed store operation and a small cell area, with a low-VDDmin SRAM operation to save dynamic power.

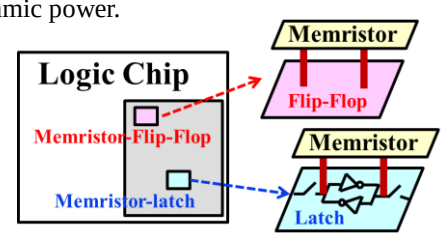


Fig. 3. Memristor-based nonvolatile latch and flip-flops.

4. Conclusions

Reducing both the power consumption and thermal stress further is a remaining challenge for 3D-ICs. By integrating the RRAM macro and memristor-based circuits in 3D-ICs, the power consumption and thermal stress can be further reduced.

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