Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1055-1056

A Block-Parallel SAR ADC for CMOS Image Sensor with 3-D Stacked Structure

Kouji Kiyoyama[1,2], Kang-Wook Lee[2], Takafumi Fukushima[2], Hideki Naganuma[3], Harufumi Kobayashi[4], Tetsu Tanaka[3], and Mitsumasa Koyanagi[2]

[1]Dept. of Electrical and Electronics Engineering, Nagasaki Institute of Applied Science
536 Aba-machi, Nagasaki, 851-0193, Japan
Phone: +81-22-795-6256, E-mail:KIYOYAMA_Koji@NiAS.ac.jp
[2]New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan
[3]Graduate School of Biomedical Engineering, Tohoku University, Japan
[4]Association of Super-Advanced Electronics Technologies (ASET), Japan

1. Introduction

Various techniques have been proposed for high-speed image sensor. These sensors require both high-sensitivity and high-resolution. Digital pixel sensor (DPS) is very attractive since the pixel performance can be significantly improved with scaling-down the size of MOSFET [1-2]. A DPS integrates an analog to digital converter (ADC) into each pixel resulting in a high speed A/D conversion. The DPS with an in-pixel ADC provided a very high frame rate of 10000-frames/s in 352×288 pixels which was fabricated by a 0.18-μm CMOS technology [3]. However, a number of MOSFETs are required for each pixel, hence the chip size increases and the resolution decreases. To realize high speed CMOS image sensor without scarifying the resolution, we have proposed a block-parallel image processing system with a three-dimensional (3-D) stacked structure [4, 5]. The eventual target of our image processing system is to develop parallel analog to digital conversion and digital readout at rate of 10000-frames/s with a pixel number of 2-MPixel. In this paper, we describe the fundamental study of block-parallel ADC. ADC designed in the test chip for evaluation employed the time interleaved successive approximation (SAR) technique.

2. Image Processing System with 3-D stacked structure

The conceptual diagram of the 3-D image processing system is illustrated in Fig.1. The proposed system consists of five layers of image sensor, correlated double sampling (CDS) array, A/D converter (ADC) array, frame memory array, and processing element array. In proposed analog block-parallel system, one block consists of 3 stacked layers which are 99 pixels image sensor, analog CDS circuit, and one ADC. Each circuit layer is stacked and electrically connected vertically using Through Si Vias (TSVs) and micro bumps, which can improve sensor performance. The 3-D structure can also improve the I/O bandwidth between image sensor and image processing element with the block-parallel processing.

3. Pixel circuit for Global Shutter

The configuration of one image sensor block with 3-D stacked layers which include 99 pixels, one CDS, and one ADC, respectively. The pixel consists of photo diode (PD), pixel select transistors (PS), a transfer gate transistor (TG), a source follower amplifier (SF), a reset transistor (RT), and photodiode reset transistor (AB). The floating diffusion capacitor (C_{FD}) for global shutter consists of the parasitic capacitance associated with the gate of SF and the drain diffusion of the TG. The pixel block and CDS are connected by TSV formed in the image sensor chip. However, the area of TSV gives rise to chip size penalty and a limited size PD area because TSV and the PD cannot be overlapped. Therefore, a TSV is shared by 99 pixels. Our system can cancel the Fixed Pattern Noise (FPN) using CDS circuit. The one pixel block area is 100×100μm^2 and TSV size is around 5μm in diameter.

4. ADC for Block-parallel signal processing

In the high-speed CMOS image sensor, ADC can be integrated at the chip level, at the column level, or pixel level. In the chip level approach, a single high-speed ADC operating at 100MS/s or more is used. To realize low power dissipation, the column level approach is used. These ADC are operated in parallel, therefore low to medium speed ADC architectures can be employed. For example, single-slope ADC, algorithmic ADC, oversampling delta-sigma ADC, and successive approximation ADC are used. On the other hand, the proposed block-parallel system requires ADC with extremely small circuit area and low power dissipation. Therefore, the trade-off among area, power dissipation, and conversion speed is important factor. The ADC used in our system is an architecture of the hybrid charge-redistribution SAR. The reason for employing this type of ADC is due to the small circuit area and low power. Fig. 2 shows the circuit schematic of the SAR ADC. The proposed ADC consists of comparator with a built-in offset voltage canceller, control logic (SAR logic), two sets of capacitor-switch array and ladder resistors. It is designed 9-bit resolution with 5-bit capacitor and 4-bit resister array. The proposed ADC has been achieved in a small circuit area of 95×100μm^2. Although a conventional SAR algorithm usually gives medium speed, our new algorithm can provide a high speed conversion by using two sets of capacitor-switch array and time interleaved method. Fig.3 shows the configuration of proposed ADC unit. The ladder resistor, reference circuit and timing controller for SAR logic are shared by eight ADCs. The total circuit area for a set of ADC unit is 800×100μm^2. Consequently, the equivalent area of one ADC occupies 100×100μm^2. Thus we achieved a very small size ADC by using the proposed configuration. A proposed ADC is designed and fabricated in 90-nm one-poly nine-metal CMOS technology. A chip photograph of the test chip is shown in Fig.4. The designed test chip consists of a four sets of ADC unit (i.e.32 ADCs). The power dissipation of the SAR ADC was very low as 381μW at supply voltage of 1.0V and sampling rate of 4MS/s. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) at temperature of 0, 25 and 85 degrees Celsius are shown in Fig. 5. The DNL is the range of -1.33 / 1.97 LSB whereas the INL is within -2.67 / 3.93 LSB. Thus it was confirmed that the requirements for DNL and INL were also satisfied in our proposed ADC.

5. Conclusions

This paper presents a very small circuit area SAR ADC.

The proposed ADC was fabricated in 90-nm CMOS technology. The fundamental tests confirm that the proposed 9-bit ADC achieved extremely low power consumption less than 0.4mW with 1.0V supply voltage, 4 MS/s conversion rate and small circuit area (100×100μm^2).

Acknowledgements

This work was entrusted by NEDO "Development of Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology." project and partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys Inc., Cadence Design System Inc., and Mentor Graphics Inc. The LSI chip used in this study has been implemented in the academy chip fabrication program of TSMC Cybershuttle service.

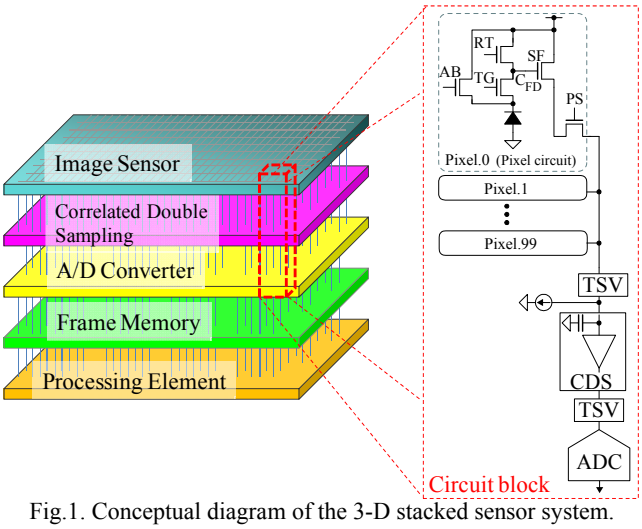

Fig.1. Conceptual diagram of the 3-D stacked sensor system.

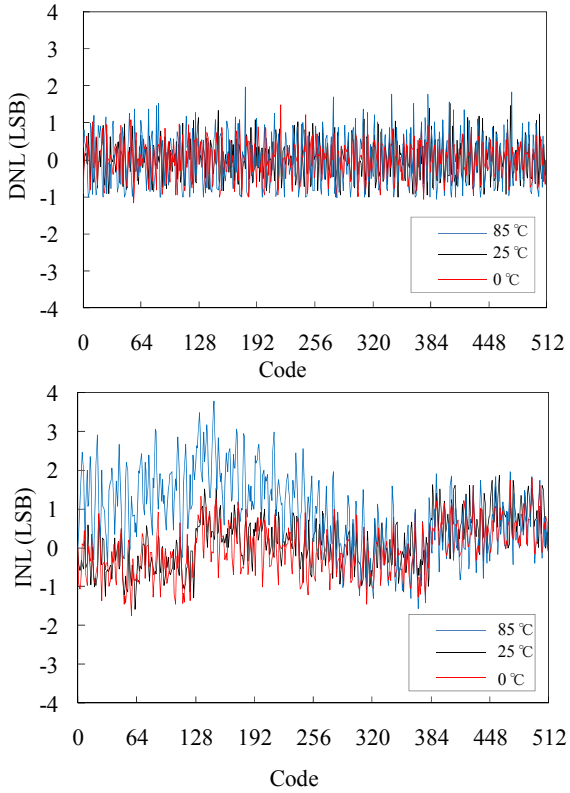

Fig.5. Measured DNL and INL

References

[1] X. David, D. Yang, Boyd Fowler, and Abbas El Gamal, "A nyquist-rate pixel-level ADC for CMOS image sensors," *IEEE J.Solid-State Circuits*, vol.34, no.3, pp.348-356, 1999.

[2] A. Kitchen, A. Bermak, and A. Bouzerdoum, "A digital pixel sensor array with programmable dynamic range," *IEEE Trans. Electron Devices*, vol.52, no.12, pp.2591-2601, 2005.

[3] S. Kleinfelder, S. Lim, X. Liu, A. EL Gamal, "A 10,000 frames/s CMOS digital pixel sensor," *IEEE J.Solid-State Circuits*, vol.36, pp.2049-2059, 2001.

[4] T.Sugimura et al., "Design of parallel reconfigurable image processor with three-dimensional structure," *IEICE Trans. Information and Systems* [in Japanese edition], J89-D6, pp.1141-1152, 2006.

[5] K. Makita, et al, *Japanese Journal of Applied Physics*, 48 (2009) 04C077.

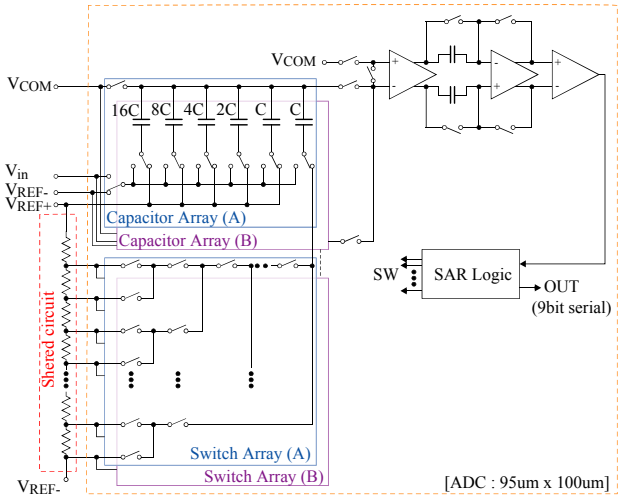

Fig.2. Circuit diagram of SAR ADC.

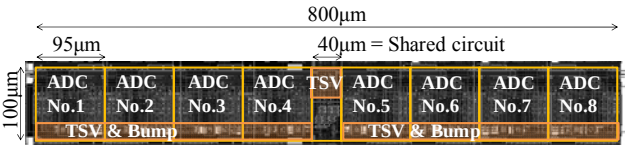

Fig.3. Layout of SAR ADC unit.

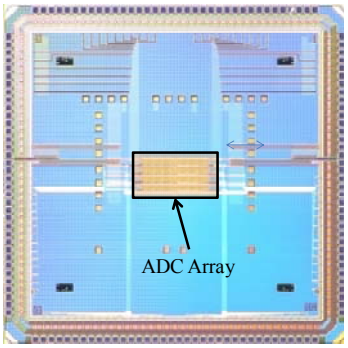

Fig.4. Photograph of the test chip.

Table I Characteristics of SAR ADC

Technology	CMOS 90 nm 1P9M
Resolution and Conversion rate	9 bit , 4MS/s
Power supply and consumption	1.0V , 381 μW
INL	-2.67 / 3.93 LSB
DNL	-1.33 / 1.97 LSB
Circuit Area	100 × 100 μm^2