Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1057-1058

Adaptive Through-Silicon-Via Control with Clustering for 3D Solid-State-Drive Boost Converter System

Koh Johguchi, Teruyoshi Hatanaka and Ken Takeuchi
Univ. of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

1. Introduction

Today, NAND flash memory based solid-state-drives (SSDs) are widely used for mobile applications instead of hard-disk-drives (HDDs). Thus, 3D-SSD system with an on-board 20-V booster has been proposed in [1-3] to increase storage capacity in a package. The booster generates the program voltage of 20 V from the supply voltage of 1.8 V. This technique enables to remove a charge pump circuit in each NAND chip [1]. However, since the performance of the boost converter is sensitive to parasitic parameters, the proposed 3D-SSD system should be carefully designed. The parasitic resistors (R_{TSV}) and capacitors (C_{TSV}) of TSVs degrade the rise-time (T_{rise}) and energy dissipation (E_{rise}) [2, 4].

On the other hand, to achieve high speed access, the number of activated NAND flash memory chips (N_{act}), is increased for sequential data access. Since increased number of activated NAND chips may cause higher power consumption, the access speed of SSDs is limited by the power budget [5]. Additionally, N_{act} is dynamically changed and most of write accesses are random accesses (4KB or less) in actual systems [6]. Therefore, we present an adoptive design methodology of the 3D-SSD system with TSVs to be compatible with every load cases. In this paper, the optimization method of the parasitic parameters of TSVs is discussed under different the load conditions. As illustrated in Fig. 1, the clustering method is proposed for Cu-TSV case to reduce the capacitance effects of TSVs. Additionally, for poly-Si TSV case, adaptive wire-line control with the TSV-number controller can optimize the performance for each load conditions.

2. Proposed 3D-SSD System with TSV technology

A. 3D-SSD with clustering and Cu-TSVs for multi-chip load

Fig. 2 shows the energy dissipation of the 20-V booster for light load (N_{act} = 1, random access) and heavy load cases (N_{act} = 32, sequential data access). In a heavy load situation, large current flows through TSVs during boosting and R_{TSV} may degrade the performance. Therefore, the diameter of TSV is more than 5.0 µm. However, for random data access (N_{act} = 1), C_{TSV} of inactivated chips may negatively affect to the performance. Thus, the 3D-SSD system with two different sizes of TSVs and cluster structure is presented as depicted in Fig. 3. A smaller TSV (TSV_{local}) is used for local connection and clusters with a switch are connected with global TSVs (TSV_{global}).

Additionally, the number of activated chips in each cluster is averaged with NAND controller. Table I compares the conventional TSV connection (non-cluster) and the proposed cluster-structure for the worst cases of heavy and light load conditions. The peak current for V_{pgm} depends on the load size which corresponds to N_{act}. Fig. 4 shows the efficiency of the proposed clustering from the SPICE simulation. In the SPICE simulation, the number of stacked chips, thickness of Si-substrate, the distance of each chip and the thickness of dielectric (SiO_2) are 128 chips, 50 µm, 50 µm and 100 nm, respectively. The cluster structure is assumed by 4 chips in each cluster and 32 clusters. In Fig. 3, Cu-TSVs are used and the diameters of TSV_{local} (ϕ_{TSVl}) and TSV_{global} (ϕ_{TSVg}) are 5.0 µm, which is sufficiently large value from the simulation. By controlling the switches and reducing parasitic capacitors, T_{rise} and E_{rise} are reduced by 37 % and 41 %, respectively, in the case of light load "random" write condition (N_{act} = 1) with the proposed structure. In addition, for the heavy load (N_{act} = 32) condition, T_{rise} and E_{rise} are also improved by ~6 % and ~5 %, respectively, due to the distributed current, despite the 2 % performance degradation by additional switches.

Fig. 5 gives the dependency of ϕ_{TSVl} for the heavy load case. The rise time is independent of ϕ_{TSVl} if ϕ_{TSVg} is sufficiently large (5.0 µm). Thus, 1.0 µm is enough size for local connection since TSV_{local} pass through only 4 chips. Consequently, a 1.0 µm TSV is the optimum size of TSV_{local} because of the area penalty, which is defined by the square of the minimum pitch ($2\phi_{TSV}$).

B. 3D-SSD with poly-Si-TSVs and TSV-number controller

A via-first technology with poly-Si TSVs is realizable without the contaminations [7, 8] although the resistance value becomes higher. Since the diameter of a poly-Si TSV is limited by less than 2.5 µm due to their low deposition rate, low TSV resistance is achieved by increasing the number of TSVs [8]. The performance of 3D-SSD, however, may degrade due to large total surface area of TSVs compared with large ϕ_{TSV} case [4]. As well as Fig. 5, sufficiently large via-numbers of TSV_{local} (N_{TSVl} > 4) can prevent the performance degradation with poly-Si TSVs. On the other hand, from the result of Fig. 6, there is the optimum number of N_{TSVg} for each load condition. As increasing N_{act}, the optimum N_{TSVg} has been shifted to larger value. Therefore, the 3D-SSD with a TSV-number controller is proposed to control the wire-line adaptively for poly-Si TSVs as shown in Fig. 7. In order to select the optimum N_{TSVg}, the TSV controller changes the number of the global TSVs by controlling the switches. The local cluster switch is controlled by these control signals and the cluster enabling signal. Therefore, the additional cost of a NAND chip is only one signal TSV (~ 100 µm^2) since the signal TSV should be high-speed connection. Fig. 8 gives the performance improvements of the proposed method with poly-Si TSVs. The proposed controller achieves 7.5 % rise-time reduction in heavy load condition (N_{act} = 32) and 16.5 % energy reduction in the case of N_{act} = 1, compared to the fixed TSV number (N_{TSVg} = 16).

C. Perfomance Estimation of Proposed 3D-SSD Application

Fig. 9 shows the advantages of the proposed 3D-SSDs for real systems. The data pattern is assumed by Windows applications [6]. In PC application, random data accesses account for >70 % of the total access as shown in Fig. 9(a). In addition, the proposed method is useful not only for the worst case of sequential data but for random data. Hence, by using cluster structure, the performance of the 3D-SSD with Cu-TSV is improved by ~10%. Furthermore, with the TSV-number controller, the performance is increased up to 2 times for poly-Si TSV case.

3. Conclusion

Table II summarizes the simulation results, which compares the proposed cluster and conventional non-cluster structures. Using the cluster structure and two sizes of Cu-TSVs, a 3D-SSD can be realized with 8.7 µsec rise-time and 1.1 µJ energy dissipation for sequential data access. Moreover, our proposal achieves ~34% rise-time and ~40 % energy reduction for random data access compared to the conventional non-cluster structure. For another scenario, poly-Si can be used for TSVs. By using a proposed TSV-controller, 7.5% of rise-time reduction in heavy load condition (N_{act} = 32) and 16.5 % energy reduction in the case of N_{act} = 1 are achieved compared with the fixed TSV number.

Acknowledgements

This work was partially supported by CREST/JST. The boost converter chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc. and Mentor Graphics, Inc.

References

[1] K. Ishida, *et al., Dig. Tech. Papers, IEEE ISSCC*, (2009) 238.
[2] T. Yasufuku, *et al.*, IEICE Trans. Electron., **E93-C**, **3**, (2010) 317.
[3] T. Hatanaka, *et al., Dig. Tech. Papers, IEEE Symp. VLSI Circuits*, (2010), 233.
[4] K. Johguchi, *et al.*, IEEE Trans. CPMT, **1**, **2**, (2011) 269.
[5] K. Takeuchi, IEEE JSSC , **44**, **3**, (2009) 1227.
[6] http://download.microsoft.com/download/5/e/6/5e66b27b-988b-4f50-af3a-c2ff1e62180f/cor-s530_wh08.pptx
[7] M. Kawano, *et al.*, IEEE Trans. Electron Devices, **55**, **7**, (2008) 1614
[8] Y. Kurita, *et al.*, IEEE Trans. Advanced Packaging, **32**, **3**, (2009) 657.

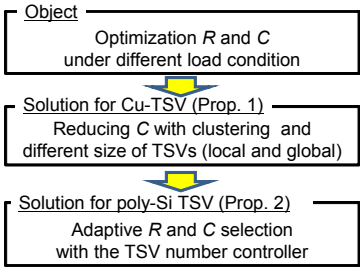


Fig. 1 The strategy of TSV design for the proposed 3D-SSD system. To reduce the effect of parasitic capacitors (C), the clustering method with two different sizes of TSVs is adopted in the case of Cu-TSV. Furthermore, the adaptive TSV number control is needed for poly-Si case to optimize the performance.

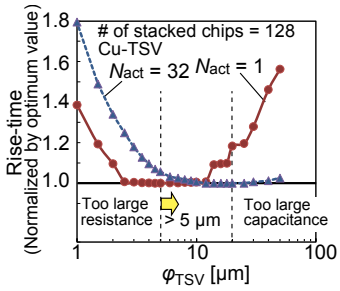


Fig 2 Rise-time for random data access (N_{act}=1) and sequential data access (N_{act}=32). In the case of N_{act}=32, the diameter of a TSV (ϕ_{TSV}) should be larger than 5 μm. However, too large ϕ_{TSV} degrades the performance for small N_{act} due to large capacitance value.

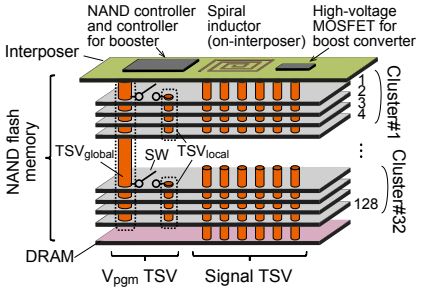
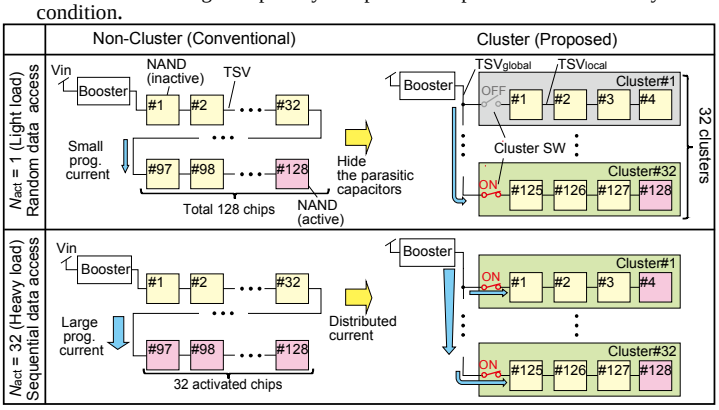


Fig. 3 Proposed 3D-SSD with clustering and two different sizes of TSVs. The local TSVs (TSV_{local}) connect NAND chips in a cluster and the global TSVs (TSV_{global}) make the connections among clusters. In this work, the 3D-SSD system has 32 clusters with 4 NAND flash memory chips in each cluster.

Table I Worst case conditions of non-cluster and cluster structure for heavy and light load situations. The number of stacked NAND chips, the number of NAND chips in a cluster (N_1) and cluster number (N_2) are assumed as 128, 4 chips and 32 clusters, respectively. For light load case, the load capacitance is reduced by cutting off the switches. Furthermore, small via size (TSV_{local}) contributes reducing area penalty and parasitic capacitance for the heavy load condition.



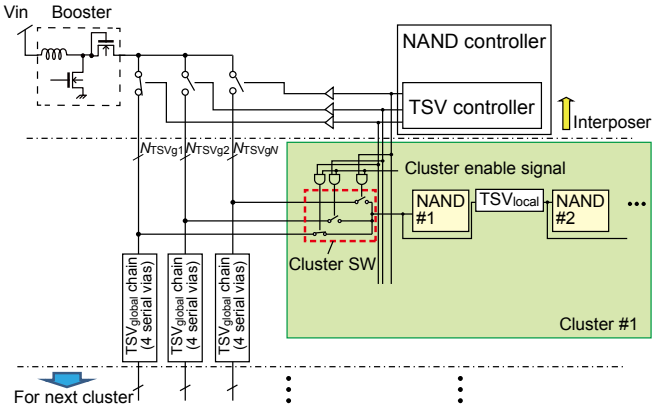
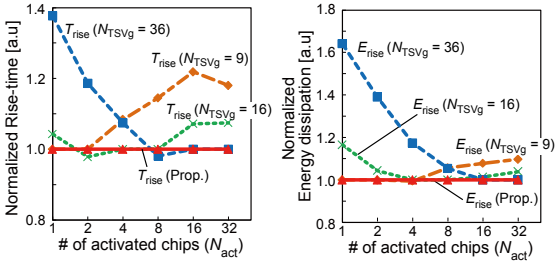


Fig. 7 Schematic diagram of the proposed TSV controller for parallel write operation. The TSV-controller dynamically selects the optimum number of TSV connected to global lines for each parallel number (N_{act}).



(a) Rise-time (b) Power dissipation

Fig. 8 Performance improvement with the proposed TSV number control for poly-Si TSV case. The vertical axis is normalized by the proposed method.

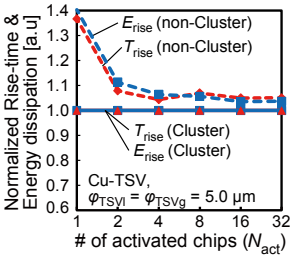


Fig. 4 Efficiency improvement by the proposed clustering TSV scheme. The proposed clustering improves the performance up to 40 % by reducing parasitic capacitors. Even if N_{act} = 32 (sequential data access) the performance is also improved due to distributed current.

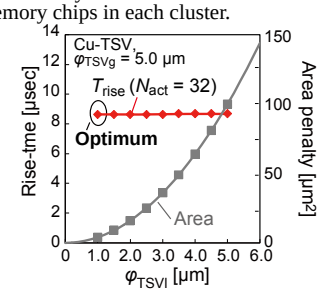
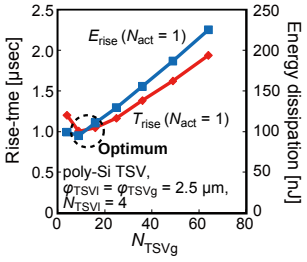
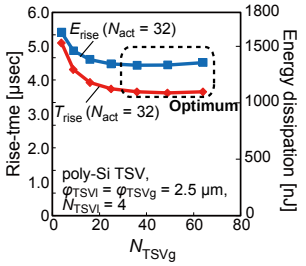


Fig 5 Dependence of rise-time on diameter of a TSV_{local} (ϕ_{TSVl}) for the heavy load and Cu-TSV case. Even if N_{act} = 32, a small TSV is sufficient for TSV_{local} due to clustering. Therefore, the optimum is ϕ_{TSVl} = 1.0μm due to area penalty of TSV_{local}, which is defined by square of $2\phi_{TSVl}$ include the margin for fabrication.

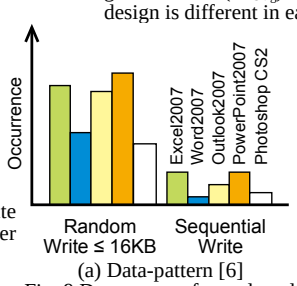


(a) N_{act} = 1

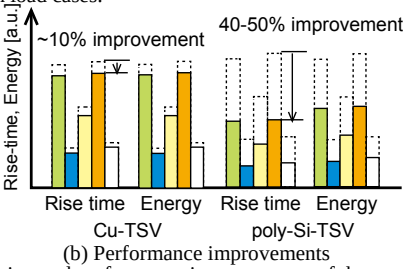


(b) N_{act} = 32

Fig. 6 Rise-time and energy simulated dependence on the number of global TSVs (N_{TSVg}) for poly-Si TSV case. The optimum TSV design is different in each load cases.



(a) Data-pattern [6]



(b) Performance improvements

Fig. 9 Data-pattern for real application and performance improvements of the proposed 3D-SSD with cluster structure.

Table II Summary of the 3-D SDD systems with TSV technology.

TSV type		Cu-TSV		poly-Si TSV		
Structure type		non-cluster (Conv.)	cluster (Prop. 1)	non-cluster (Conv.)	cluster (Fixed via #)	cluster w/ TSV ctrl. (Prop. 2)
ϕ_{TSVg} / ϕ_{TSVl} [μm]		5.0 / -	1.0 / 5.0	2.5 / -	2.5 / 2.5	2.5 / 2.5
N_{TSVg} / N_{TSVl}		1 / -	1 / 1	36 / -	4 / 16	4 / (9,16,36)
Area penalty for TSVs[μm^2]		~ 100	**~ 104**	~ 900	~500	~ 1,100
Rise-time [μsec]	N_{act} = 1	0.59	**0.44**	1.94	1.06	**0.59**
	N_{act} = 32	9.13	**8.68**	14.9	11.8	**9.13**
Energy [nJ]	N_{act} = 1	74.2	**52.9**	199.7	110.4	**74.2**
	N_{act} = 32	1,147	**1,107**	1,567	1,382	**1,147**