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An Injection-Locked LC Frequency Divider to Achieve Wide Locking Range and Low Power Consumption

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1. Introduction

Most wireless systems are narrow band architecture. Therefore, the analog LC-based frequency divider shows a promising topology to implement into a modern wireless transceiver. The design challenge of analog divider must achieve simultaneously the low power dissipation and wide locking frequencies. To achieve this goal, a topology uses both approaches including the in-phase injection and a lossy path to decrease tank current in this work. The proposed topology was fabricated using TSMC 0.18μm CMOS technology. The measurement demonstrates the proposed divider operates the input frequency from 12~18GHz, and has a 6 GHz locking range dissipates 4.4mW DC power.

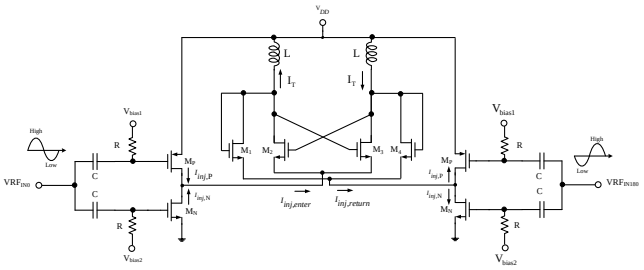


Fig. 1 Proposed ÷2 circuit schematic, the relative current direction of injection and return currents is depicted by the arrows.

2. Proposed topology to enhance locking range

The proposed injection locking circuit using two in-phase signals to enhance the lock range is shown in Fig.1. The input differential voltages ($VRF_{IN,0}$ and $VRF_{IN,180}$) convert to current signal ($I_{inj,P}$ and $I_{inj,N}$) using both the M_P and M_N transistors. The two currents are added to compose the injection signals ($I_{inj,enter}$ and $I_{inj,return}$), which inject into the divider via the M_2 and M_3 transistors and return from the divider using the M_1 and M_4 transistors. The input current ($I_{inj,enter}$) injects into a cross-pair (M_2 and M_3) transistor to accomplish the ÷ 2 operation, the return current ($I_{inj,return}$) leaves out from the diode-connected M_1 and M_4 transistors. The free run frequency is determined by the inductor and parasitic capacitor inside the LC tank.

Furthermore, the proposed topology also dissipates low power since the adoption of current bleeding in the M_N and M_P transistors. The use of the M_N and M_P transistors not only has the in-phase injection but also has the current bleeding behavior as shown in Fig.1. The current bleeding topology is modified from mixer architecture [3]. The PMOS transistor (M_P) supplies the DC current in prototype mixer design. The proposed divider uses the M_P transistor to supply both DC and RF signals, the DC-RF conversion

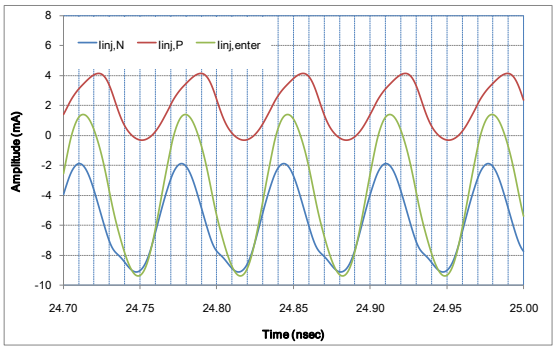


Fig.2 Simulation waveform of $I_{inj,enter}$, $I_{inj,N}$ and $I_{inj,P}$ currents

efficiency is enhanced to decrease the power dissipation. When the injection currents at a frequency $\omega_{inj,enter}$ locks the oscillator, the tank current includes the injected current and output current. The $I_{inj,enter}$ current includes two components, the $I_{inj,N}$ and $I_{inj,P}$ currents which inject into the differential-pair connection of the NMOS and PMOS transistors at input path.

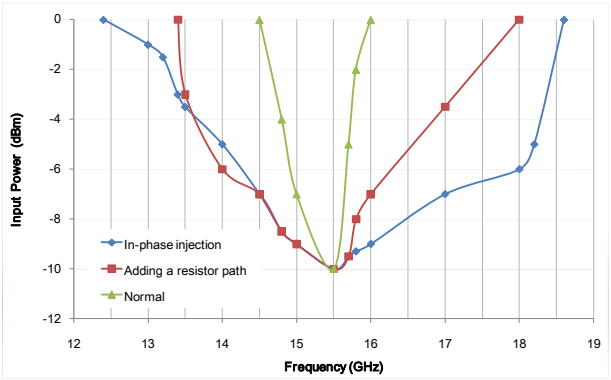


Fig.3 Comparison of input sensitivity including normal, leakage path, in-phase injection curves.

The in-phase behavior of both injected currents is obtained since the NMOS and PMOS transistors are composed a switch connection. The simulation of both $I_{inj,N}$ and $I_{inj,P}$ waveform is shown in Fig.2, which illustrated the in-phase injection of both currents in this graph. Hence, the total input injection current is enhanced due to the summation of both currents. To compare the locking range with different topologies such as adding a loss path and in-phase injection, the input sensitivity is simulated for these two approaches as depicted in Fig.3. In which the normal condition depicts the injection without previous two techniques. The locking range is defined by the frequency range when the input power achieves to 0 dBm. Apparently, the locking ranges are improved 4.7 GHz by utilizing in-phase injection

and 1.6GHz by adding a loss path.

3. Measurement results

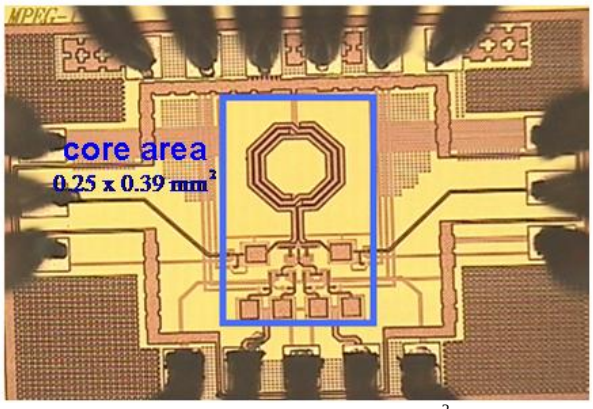
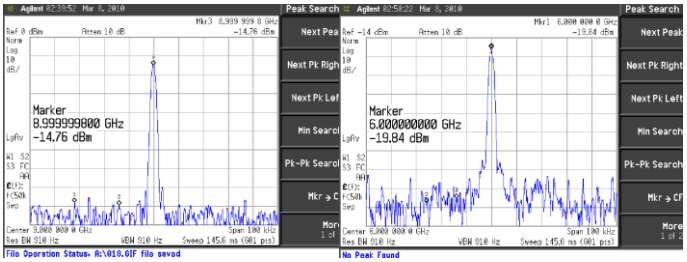
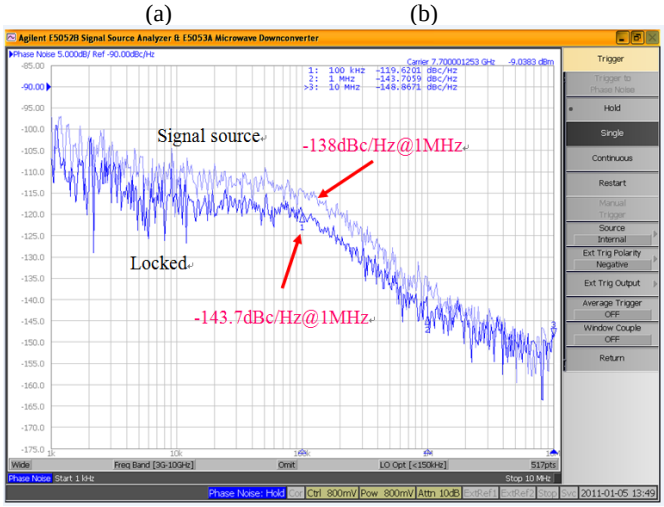


Fig.4 Chip photo graph, total area 700 x 900 μm^2 and core area 250 x 390 μm^2



(a) (b)



(c)

Fig. 5(a) Measured spectrum of upper band frequency.
Fig. 5(b) Measured spectrum of lower band frequency.
Fig. 5(c) Comparison of measured spectrum for both curves, free run and injection-locked curves

To verify the proposed topology, a circuit has been designed and fabricated using TSMC 0.18μm CMOS technology. The chip photo is depicted in Fig.4, where the total chip area is 0.7 x 0.9 mm^2 and the core area is 0.25 x 0.39 mm^2. The measurement setup adopts Agilent Signal Generator, Spectrum Analyzer E4440A, Signal Source Analyzer E5052B, and Power Supply E5270B. Use a six pins DC probe to supply 0.8V voltage, the RF source swept from 12GHz to 18GHz is excited into the input pad. The output signal with upper and lower frequencies were recorded by using a spectrum as depicted in Fig.5a and 5b, respectively. The spectrum recorded the lower and upper output frequencies with 6GHz and 9GHz, respectively. Hence, the proposed divider has 6GHz locking range at input terminal and dissipates DC power of 4.4 mW. Moreover, the comparison of the phase noises with locked and free-run spectrum is depicted in Fig.5(c). Apparently, the difference of phase noise at 1MHz is 5.7 dBc/Hz which is approximately to the ideal value of 6 dBc/Hz [5].

Table I Benchmark of proposed topology with reported work

Comparison		This	Ref.[4] 2009	Ref.[3] 2008	Ref.[2] 2005	Ref.[1] 2004
Technology		0.18um CMOS	0.18um CMOS	90nm CMOS	0.13um CMOS	0.13um CMOS
Input Frequency (GHz)		15	10	60	38	40
Locking Range	(GHz)	6	3.8	4.4	3.5	1.5
	(%)	40.00	38.00	7.33	9.21	3.75
Power Dissipation (mW)		4.4	9.02	5	12	3
FOM	(GHz/mW)$^{\&}$	1.36	0.42	0.88	0.29	0.50
	(% / mW)$^{\#}$	9.09	4.21	1.47	0.77	1.25

FOM (GHz / mW)$^{\&}$ =LR(GHz)/ PD(mW)
FOM (% / mW)$^{\#}$ = LR(%) / PD(mW)

Table I compares the performance of proposed circuit with reported papers in terms of input frequency, locking range, power consumption and Figure-of-Merit (FOM), which is defined by the locking range divided by power consumption. Notably, the locking range column is expressed by both the locked frequency and the percentage of locked frequency divided by the input frequency. Therefore, the FOM also has two columns to fairly compare with previous work. The result demonstrates the proposed topology not only has the low power consumption but also has the wide locking range. The corresponding FOM achieves the excellent value in this column. The result is predictable since the adoption of two techniques in the proposed topology.

4. Conclusions

A new ÷2 topology incorporated with in-phase injection and adding a loosy resistor in return path has been proposed to enhance the locking range and dissipate low DC power. To demonstrate the proposed circuit, the chip was manufactured by TSMC 0.18μm CMOS technology. Measurements show the divider not only has 6GHz locking range swept input frequency from 12GHz to 18GHz but also dissipates 4.4mW. Results of this work provide a valuable reference to design a ÷2 circuit for wireless communication.

References

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