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A 0.1-V 13-GHz Transformer-Based Quadrature VCO with a Capacitor Coupling Technique in 90nm CMOS

Tatsuya Kamimura, Sang_yeop Lee, Satoru Tanoi, Hiroyuki Ito, Noboru Ishihara and Kazuya Masu

Solutions Research Laboratory, Tokyo Institute of Technology
4259-S2-14 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan
Phone: +81-45-924-5031 E-mail: paper@lsi.pi.titech.ac.jp

1. Introduction

A low power RF circuit is strongly demanded by sensor and healthcare systems. High-microwave band is attractive for such applications because antenna size can be easily reduced. This paper proposes a high-microwave-band quadrature VCO (QVCO) that operates under 0.1 V power supply to save power. The conventional QVCO with current sources [1] is generally difficult to achieve enough negative conductance under low supply voltage. Thus, transformer feedback and body bias coupling techniques have been reported [2,3]. However, it is still a challenge to obtain sufficient transconductance g_m at high-microwave band. The present work introduces the capacitor coupling technique to boost g_m of the transformer feedback QVCO. The prototype QVCO is fabricated by using 90 nm Si CMOS technology, and measured performances are discussed.

2. Low-Supply-Voltage QVCO

Fig. 1 shows the proposed QVCO. Low power supply operation at high-microwave band is achieved by leveraging two techniques: transformer feedback and capacitor coupling.

It has been reported that a transformer feedback can enhance signal swing even though the cross-coupled transistors (M_1, M_2, M_3 and M_4) have low transconductance g_m [2]. This work exploits it and introduces capacitor coupling technique for achieving quadrature operation and g_m boosting at higher frequency operation. Signals at the drain terminals are injected to the source terminals through capacitors C_c. The injected signals on source terminals have 90 degree phase shift and are amplified by common-gate amplifier operation. Capacitors C_g and resistors R_g are used to feed gate bias voltage independently for low supply voltage operation.

The square-shaped spiral transformer as shown in Fig. 2 was designed. A top thick metal layer is used for achieving higher Q-factor. Table I shows simulated inductance (L_p, L_s), Q-factor (Q_p, Q_s) and coupling coefficient of the trans-former k at frequency of 13 GHz. Dimensions were optimized by using a 2.5D electro-magnetic-field analysis.

3. Measurement Results

Fig. 3 shows a chip micrograph of the proposed QVCO. The QVCO area is 800 um × 250 um including signal output buffers for testing. The measured frequency tuning ranges were 13.06-13.12 GHz and 13.17-13.22 GHz at power supply voltages of 0.1 V and 0.2 V, respectively, with V_{bias} =0.4 V. The power consumption of the QVCO core were 0.68 mW and 2.8 mW, respectively, when the varactor control voltage was equal to the supply voltage (V_{ctrl}=V_{dd}). Fig. 4 shows phase noise characteristics at f_o =13 GHz under free-running condition. Phase noises of the QVCO at 1MHz offset were -94 dBc/Hz and -100 dBc/Hz at supply voltages of 0.1 V and 0.2 V, respectively. Fig. 5 shows frequency spectrum of the VCO output at f_o =13 GHz. Low carrier power with the high system noise is because of limited frequency range of test buffers.

Performances of the proposed QVCO are summarized in Table II with the previously reported VCOs. The proposed QVCO achieves high-frequency operation under 0.1V power supply. Power consumption is 0.68 mW and is comparable with other low-supply-voltage VCOs. A figure of merit (FoM) on the phase noise ($L(\Delta f)$), the output frequency (f_o), and the power consumption (P_{diff}) are also estimated. FoM is expressed as

$$FoM = L(\Delta f) - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{diff}}{1\mathrm{mW}}\right) \qquad (1)$$

Measured FoM values were -178 dBc/Hz with 0.1 V and 0.2 V power supply.

4. Conclusions

This paper proposed the transformer-feedback QVCO with capacitor coupling technique for boosting g_m at high frequencies. The prototype QVCO in 90 nm Si CMOS achieved 13 GHz operation under low power supply voltage of 0.1 V with typical FoM.

Acknowledgements

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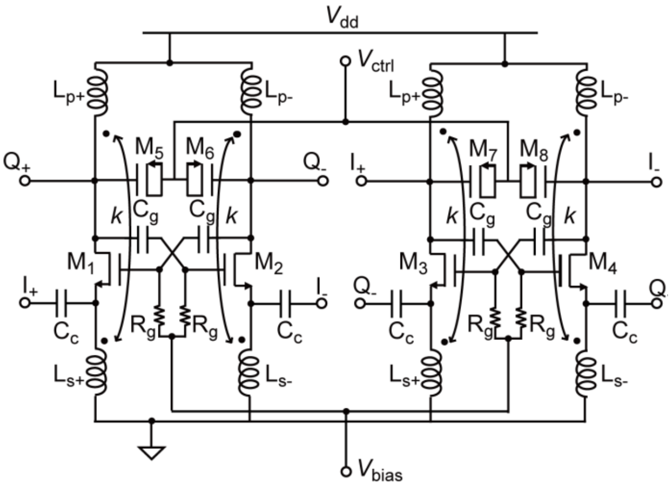

Fig. 1 Proposed QVCO with the capacitor coupling.

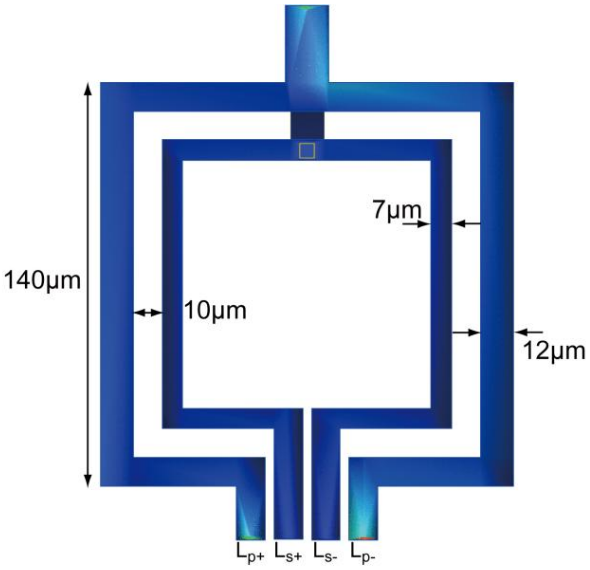

Fig. 2 On-chip square-shaped spiral transformer.

Table I Transformer Parameters at 13 GHz.

L_p	Q_p	L_s	Q_s	k
0.19 nH	17.9	0.14 nH	14.7	0.50

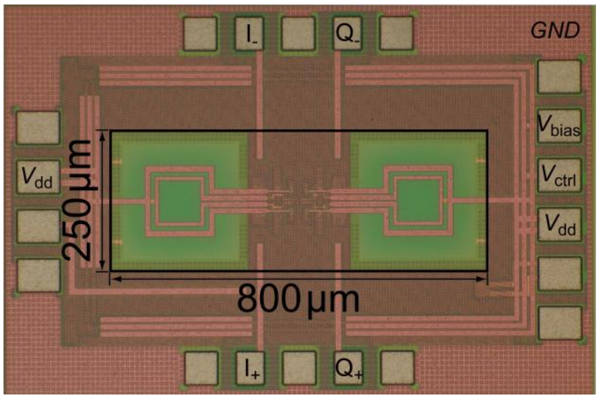

Fig. 3 Chip micrograph.

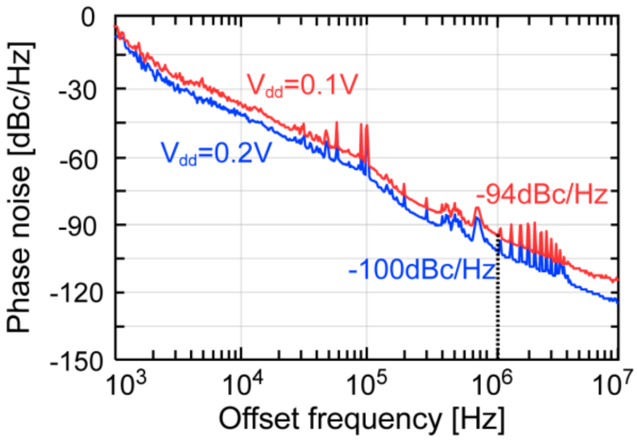

Fig. 4 Measured phase noise of the proposed QVCO when V_{dd}=0.1 V and V_{dd}=0.2 V.

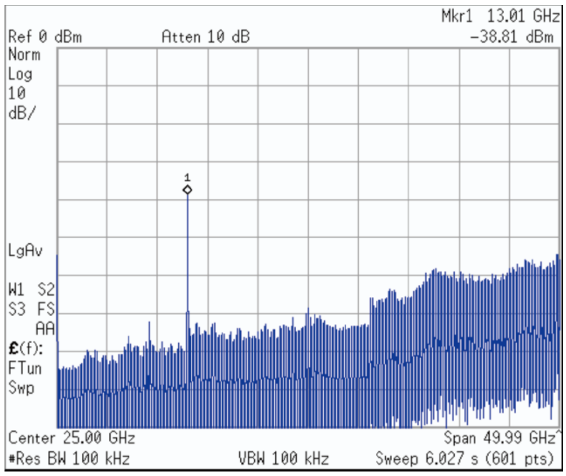

Fig. 5 Measured spectrum of the proposed QVCO when V_{dd}=0.1 V.

Table II Performance summary and comparison of LC-VCOs.

	CMOS process	f_o [GHz]	V_{dd} [V]	P_{diff} [mW]	Δf [MHz]	$L(\Delta f)$ [dBc/Hz]	*FoM* [dBc/Hz]	Area [mm^2]	IQ Output
This work	90 nm	13	0.1	0.68	1	-94	-178	0.20	Yes
	-	13	0.2	2.80	1	-100	-178	-	-
[1]	130 nm	10	1.8	N/A	1	-95	N/A	0.16	Yes
[2]	180 nm	1	0.4	1.46	1	-129	-190	0.76	No
[3]	90 nm	4	0.2	0.33	1	-113	-187	0.76	Yes
[4]	180 nm	10	1.0	10	1	-112	-182	0.88	Yes