1.2-17.6 GHz Ring-VCO-Based PLL with Injection Locking in 65 nm CMOS

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1. Introduction
A frequency synthesizer covering wide-frequency band is strongly demanded in the next universal RF systems such as software define radio (SDR) systems and cognitive radios systems. In this paper, 1.2-17.6 GHz PLL based on a ring VCO is demonstrated. To get wide tuning range, combination architecture with the ring VCO, frequency dividers, and doublers is employed. To get the low phase noise characteristics, a double PLL architecture with a reference signal injection technique is introduced [1-3].

2. Design of the Wide-Frequency-Range PLL
Following issues are considered to achieve wide-band and low-phase-noise PLLs with ring VCOs.

1. Wide-band operation: In designing PLLs, it is important to consider the VCO gain; $K_{\text{VCO}}$, because it affects the loop dynamic characteristics widely. Generally, wide-frequency tuning, and lower supply voltage with CMOS scaling cause high $K_{\text{VCO}}$, especially in ring VCOs. As $K_{\text{VCO}}$ becomes higher, PLL performances such as stability of the loop, spurious levels are degraded. Therefore, frequency dividers and mixers have been used in the PLL to get the wide band operation [4].

2. Low phase noise: In general, ring VCOs have worse phase noise than LC VCOs. To improve phase noise, a reference signal injection technique is introduced [1-3]. Furthermore, for widening the lock range of injection locking [5], the double PLL architecture has been employed to generate high-frequency reference.

Fig. 1 shows the proposed double PLL. A reference PLL generates reference signals of which frequency step is 50 MHz (300-600 MHz) to a main PLL. A main PLL generates wide-frequency range signals using a frequency doubler and dividers. Fig. 1 also shows the configuration of the main PLL, which uses a phase-locked loop for the frequency locking and injection locking for the final phase locking. Phase noise reduction is achieved by terms of this mechanism. In this paper, we implemented the main PLL part with a frequency doubler and dividers. For achieving a wide-frequency operating and minimizing the chip area; the frequency doubler which uses I/Q outputs of the ring VCO consist of pseudo-nMOS NORs (Fig.2), and dividers consist of differential pseudo-nMOS latches [6].

Fig. 3 shows a proposed two-stage differential VCO for generating I/Q outputs. A delay cell of the VCO contains an inverter latch that generates a delay by positive feedback in order to satisfy the oscillation condition. In the delay cell, the pMOS transistors into which the bias-level-shifted control bias, $I_{\text{bias}}$, are input are added in order to make the range of sensitive voltages identical to the rail-to-rail voltage range, and to maintain $K_{\text{VCO}}$ over the range [7]. In addition, nMOS switches are connected at the differential output nodes to achieve subharmonic injection locking.

3. Fabrication Results
The main PLL was fabricated by a 65 nm CMOS process, and occupies an area of 0.2 mm x 0.3 mm as shown in Fig. 4. It was measured with 1.2-V power supply. Frequency tuning range of 1.2-17.6 GHz shown in Fig. 5 was measured, when the PLL was locked only with a phase-locked loop. A 50%- duty-cycle reference signals were generated by an external pulse pattern generator. At the PLL output frequency ($f_{\text{osc}}$) of over 7.2 GHz, it was difficult to generate effective injection pulses which have enough power for injection locking [5].

Fig. 6 shows maximum output frequencies with/without injection locking, respectively. The rejection ratio between fundamental ($f_{\text{osc}}$) and frequency-doubled tones ($f_{\text{dou}}$) were -15 dB and -10 dB, respectively. Reasons why output signal levels ($f_{\text{osc}}$) are low were power losses due to probes, cables, and output buffers at over 10 GHz. The spurious levels at $f_{\text{dou}}=14.4$ GHz without/injection locking ($f_{\text{ref}}=450$ MHz) were -39 and -36 dB, respectively (Fig. 7). The phase noise of the PLL fundamental tone ($f_{\text{osc}}=7.2$ GHz) and the frequency-doubled tone ($f_{\text{dou}}=14.4$ GHz) were measured, and, with injection locking, -94 dBc/Hz and -104 dBc/Hz were observed at a 1 MHz offset (Fig. 8). Fig. 8 also shows 16-dB ($f_{\text{osc}}$) and 8-dB ($f_{\text{dou}}$) reduction with injection locking compared to phase noise characteristics without it, respectively.

4. Conclusions
A wide-frequency-range PLL architecture using the combination of a ring VCO, a frequency doubler, and dividers was proposed, and fabricated with 65 nm CMOS. We succeeded in obtaining 1.2-17.6 GHz wide-frequency band operation. Furthermore, 8-dB phase-noise reduction at $f_{\text{dou}}=14.4$ GHz was achieved with injection locking.

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References
[4] B. Razavi: VLSI Circuits, 2009, p. 120.
Fig. 1 Proposed injection-locked PLL.

Fig. 2 Topology of the proposed (a) NOR, and (b) frequency doubler.

Fig. 3 Topology of the proposed (a) delay cell, and (b) VCO.

Fig. 4 A micrograph of the proposed PLL.

Fig. 5 Measured output frequency of the proposed PLL.

Fig. 6 Measured output frequency spectra at (a) \( f_{\text{dou}} = 14.4 \) GHz with injection and (b) \( f_{\text{dou}} = 17.6 \) GHz without injection.

Fig. 7 Measured output frequency spectra at \( f_{\text{dou}} = 14.4 \) GHz (a) without and (b) with injection (\( f_{\text{ref}} = 450 \) MHz).

Fig. 8 Measured phase noise at \( f_{\text{osc}} = 7.2 \) GHz, \( f_{\text{dou}} = 14.4 \) GHz without/with injection locking.

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