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Asynchronous Pulse Transmitter for Power Reduction in ThruChip Interface

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1. Introduction

Inductive-Coupling Link namely ThruChip Interface (TCI) is a wireless interconnect between three-dimensionally (3D) stacked chips. An asynchronous-type TCI transceiver [1] is widely used in various applications, such as NAND Flash memory stacking [2-3], DRAM-GPU stacking [4], and non-contact memory cards [5] because of its high-speed capability and simple data recovery mechanism without use of a clock signal. However one of the technical issues is large static (DC) power consumption in the asynchronous transmitter (Tx) (Fig.1 (a)) which makes the Tx power dissipation to be dominant in the total TCI power dissipation. This power penalty becomes significant when the data rate is lowered. In mobile applications, the data rate is relatively low (<2Gb/s) and by necessity the power consumption should also be low accordingly. In this paper, an asynchronous inductive-coupling pulse Tx is proposed. It eliminates the DC power consumption and therefore exhibits linear power scalability to the data rate. As a result, power reduction to 1/4 at 1.5Gb/s and 1/60 at 100Mb/s compared to the conventional Tx is achieved. In addition, a crosstalk immune receiver is also proposed for low-power relayed transmission using the pulse Tx.

2. Asynchronous pulse transmitter

Fig.1 (b) depicts the proposed asynchronous pulse Tx. Instead of driving an H-bridge driver by differential data signal *Txdata*, delayed data signal *Delay* is used to produce intermittent pulse current I_T only at *Txdata* transition. No DC power is consumed, resulting in linear power scalability to the data rate. The I_T pulse current induces positive and negative bi-polar double pulses V_R in the receiver (Rx) coil. Although the V_R pulse waveform is varied from the conventional one, a conventional hysteresis-comparator-based Rx [2] can be used for asynchronous data recovery. By properly resetting the initial state, the Rx can ignore the first pulse in the double pulses but detect the latter pulse and thus recover digital data similarly to the conventional manner. Threshold voltage of the hysteresis Rx V_{TH} may drift due to the first pulse input. This V_{TH} drift temporarily degrades the Rx sensitivity. A time interval between the first and the last pulse should be carefully designed to guarantee the Rx long enough time for recovering the sensitivity. The time interval is determined by the I_T pulse width τ. Since shorter τ lowers the power dissipation, there is a tradeoff between power dissipation and the time margin for the Rx sensitivity recovery.

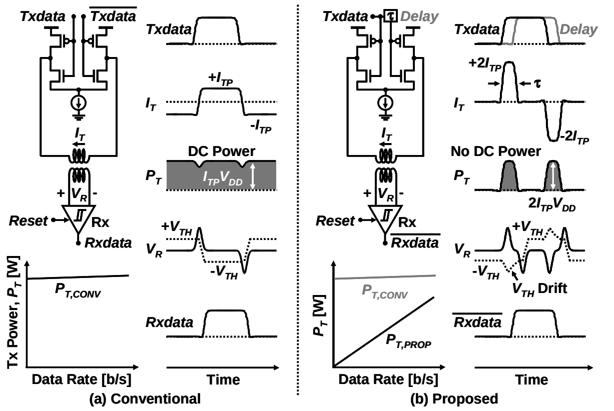

Fig.1 Circuit diagrams and operation waveforms of (a) conventional and (b) proposed pulse transmitter.

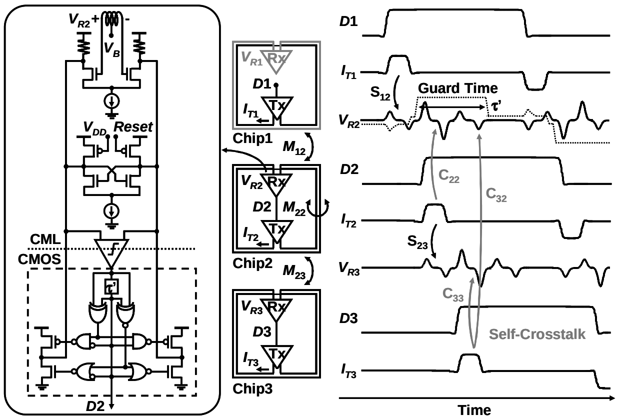

Fig.2 Receiver circuit with active self-crosstalk guard for relayed transmission.

3. Relayed transmission by pulse transmitter

In multiple-chip stacking, relayed transmission is an effective way to reduce required coil size. It is therefore widely used especially in NAND Flash memory stacking [2-3] where the number of stacked chips is typically large (e.g. 64~128). However, the proposed pulse Tx can not be used in the latest power- and area-efficient relay scheme [3]. The problem is vertical crosstalk between stacked coils. As shown in Fig.2, transceiver coils are concentrically stacked for relayed transmission. Since the coil emits magnetic field both upwards and downwards, vertical self-crosstalk is induced such as C_{22} or C_{32} in Fig.2 (like self-voice echoes). In case of the conventional Tx, the signal and the self-crosstalk in V_R each becomes a single mono-polar pulse at every data transitions. Therefore, the self-crosstalk does not toggle the received data output. In this case, data can be relayed by using the conventional Rx [4]. In the proposed pulse Tx, on the other hand, V_R becomes the

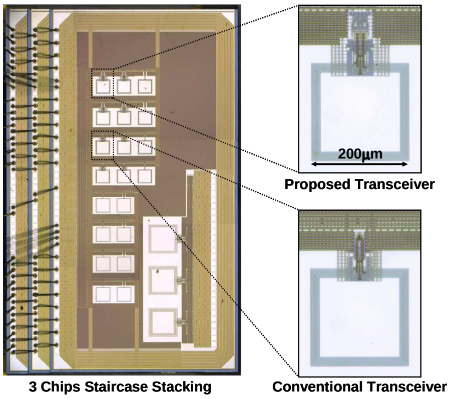

Fig.3 Stacked test chips in 0.18µm CMOS.

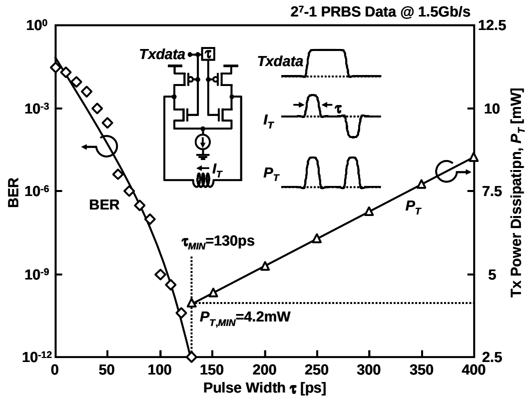

Fig.4 Pulse width τ vs. BER and Tx power dissipation.

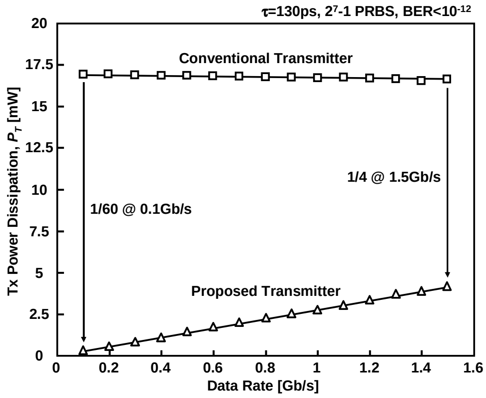

Fig.5 Data rate vs. Tx power dissipation.

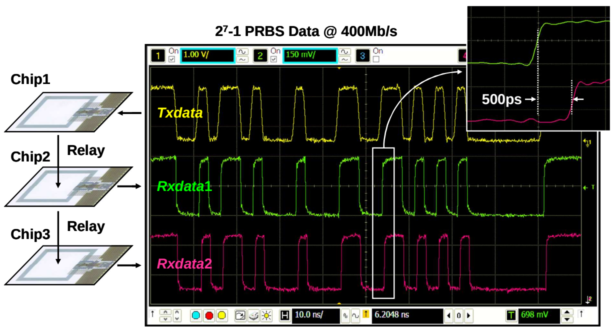

Fig.6 Snapshot of relayed data waveforms.

bi-polar double pulses. Received data will be toggled by the self-crosstalk. This would cause undesired oscillation due to positive feedback nature in this relay scheme. In order to solve this problem, an active self-crosstalk guard circuit is added to the Rx output (Fig.2). It detects received data transitions by an XOR-based edge detector and forces to hold the received data for a certain amount of time period τ'. During this guard time, the self-crosstalk is all ignored.

4. Test-chip measurement

The test chip is designed and fabricated in 0.18µm CMOS (Fig. 3). Three test chips are stacked in staircase stacking with a chip offset of around 300µm. The top two chips are thinned to 40µm-thick and the glue between the chips is 10µm-thick. Communication distance between the transceivers is therefore 50µm. Both the conventional and proposed transceivers are integrated in the test chip for comparison. The coil diameter is 200µm.

First, the minimum pulse width τ is measured to see the trade-off between the power dissipation and reliability. As it can be seen in Fig.4, the minimum τ is around 130ps for BER<10^{-12} at 1.5Gb/s operation. The Tx power dissipation at τ=130ps is 4.2mW.

Fig. 5 shows Tx power dissipation dependence on data rate. Compared to the conventional H-bridge Tx, the power dissipation in the proposed pulse Tx is reduced to 1/4 at 1.5Gb/s and 1/60 at 100Mb/s.

Relayed transmission using the pulse Tx and the self-crosstalk immune Rx is evaluated. Successful operation can be seen in a snapshot of relayed data waveforms in Fig.6. The maximum data rate and the delay per relay is measured to be 400Mb/s and 500ps respectively. The transmitter power dissipation is 1.8mW at 400Mb/s.

5. Conclusion

An asynchronous inductive-coupling pulse transmitter is proposed to eliminate static transmit current consumption. It can provide linear power scalability to the operating frequency for low-power mobile applications. Power reduction to 1/4 at 1.5Gb/s and 1/60 at 100Mb/s is achieved, compared to the conventional transmitter. Also a crosstalk immune inductive-coupling receiver is presented for low-power relayed transmission using the proposed pulse transmitter. An active crosstalk guard circuit is introduced to ignore echo-like self-crosstalk. Test- chip measurement demonstrates successful operation in relayed transmission at up to 400Mb/s.

Acknowledgements

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