A 60-GHz Band Low Power Differential CMOS LNA with Current-Reuse Topology
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1. Introduction
In the context of the scaling of CMOS technology, the possibility of realizing an all-in-one-chip CMOS millimeter-wave (mm-wave) transceiver is growing. A high-cost performance transceiver for over 1-Gbps high-speed wireless communication systems even including an antenna is attracting much attention. In [1], a bonding wire loop antenna mounted on a standard ball grid array (BGA) package was presented. This balanced antenna has advantages in terms of area and radiation efficiency compared to a single-ended one, because it has higher design flexibility. Since this antenna outputs a differential signal, following RF frontend blocks of the antenna, such as switch and low-noise amplifier (LNA), should be implemented as differential circuits. Compared to single-ended circuits, differential circuits have advantages that the ideal ac ground can be obtained easily and there is immunity to common-mode disturbances, such as leakage of LO signal [2]. However, differential circuits tend to consume more power and occupy larger area than single-ended circuits do.

In order to reduce the power dissipation of differential circuits, a differential mm-wave LNA is proposed. The proposed LNA employs current-reuse topology with gate-to-drain capacitance (Cgd) neutralization technique. The design methodology and simulated- and measured-results of the LNA are described.

2. LNA Design
Design Overview
Figure 1 shows a schematic diagram of the proposed LNA. The LNA consists of three pseudo differential common-source stages with cross-coupled capacitors. Current-reuse topology is employed to reduce the power consumption. Basic concept of the current-reuse topology for the three-stage single-ended LNA has already been proposed in [3]. That is, a dc bias current of the first stage is reused by the following two stages, i.e. \( I_{dc1} = I_{dc2} + I_{dc3} \), where \( I_{dc1} \), \( I_{dc2} \), and \( I_{dc3} \) are dc current consumed by the first, the second, and the third stage, and the whole LNA. Note that node P in Fig. 1 can be treated as an ac ground because of differential operation. Hence a large capacitor which makes the node P an ac ground is unnecessary. Additionally, large ground area for source of the second and the third stage can be minimized for the same reason. These contribute to a reduction of area consumption, and make it easier to implement the current-reuse topology compared to the single-ended case.

Dimensions of each MOS transistor are chosen such that an \( f_{MAX} \) and an NF of the transistor are maximized and minimized, respectively, for given drain-to-source current [4]. Smaller transistors are preferable in terms of power consumption, while transistors of moderate size are preferable for power and noise matching with 50-Ohm signal sources. Therefore the first stage of the presented LNA, which is expected to be matched with 50-Ohm, consists of relatively large devices and consumes as large a current as the following stages consume.

Matching circuits in the LNA consist of spiral inductors and finger capacitors. Transmission-lines are used as inter-stage connection paths. Cgd-Neutralization Technique
A reverse gain of MOSFETs decreases stability of amplifier and makes it difficult to design matching circuits operating at mm-wave frequency. In general, a cascode topology is employed in order to suppress the reverse gain [4], [6]; or a source-degeneration is used to improve stability [3]. However, in the proposed LNA, two transistors are already stacked at the dc domain; therefore, sufficient voltage margin for additional cascode devices no longer exists. Moreover, introduction of source-degeneration must result in gain decrease. The proposed LNA employs a Cgd-neutralization technique realized by cross-coupled capacitors, i.e. this can be applied only on differential circuit, in each stage in order to suppress reverse gain [5]. By using this technique, reverse gain is suppressed without additional voltage headroom and gain decrease.

Cross-coupled capacitor pairs, shown in Fig. 1 are realized by MOS capacitors, i.e. drain-source shorted MOSFETs. The dimensions of the MOS capacitors are chosen such that [S12] of each stage is minimized.
3. Simulation and Measurement Results

The designed LNA is fabricated in a 65-nm standard CMOS process. The chip size including pads for measurement is 620 x 630 μm². The chip micrograph is shown in Fig. 2. Figure 3 shows measured/simulated gain (|S_{dd21}|) and NF. Figures 4(a) and (b) show measured/simulated reverse gain (|S_{12}|) and CMRR (20\log_{10}[|S_{dd21}|/|S_{cc21}|]), respectively. The LNA consumes 16 mA of dc current from a 1.2 V supply voltage. The proposed LNA shows forward gain of 18.9 dB, NF of 5.1 dB, reverse gain of less than -40 dB, and CMRR of over 20 dB at 56 GHz. The significant discrepancy in measured/simulated reverse gain is attributable to the measurement limitation of a network-analyzer used for measurements. Table 1 shows a comparison of the mm-wave LNA’s performances with those of recently published CMOS LNAs. Most LNAs are single-ended. The proposed LNA’s performances are comparable to those of the others. Furthermore, the proposed LNA offers various benefits of differential operation such as a CMRR. In addition, the proposed LNA achieved the highest FOM value among LNAs that are not single-ended, whose signal type is represented by colored fonts; where the FOM is defined as:

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FOM = \frac{\text{Gain}[\text{dB}] \times \text{BW}[\text{GHz}]}{\text{NF}[\text{dB}] - 1} \times \text{Power}[\text{mW}]
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4. Conclusions

A mm-wave differential CMOS LNA using current-reuse topology is designed and fabricated in 65-nm standard CMOS technology. The LNA overcomes the reverse gain problem by employing a C_{gd}-neutralization technique without any additional voltage headroom consumption.

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References