Low Voltage and Low power UWB CMOS LNA using Forward Body Biasing Technique

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Abstract

An ultra-wideband (UWB) low noise amplifier (LNA) was proposed and implemented using 130 nm 1.2V CMOS technology. The adoption of forward body biasing (FBB) technique in a cascode amplifier enables an aggressive scaling of supply voltage $V_{DD}$ to 0.9V and gate input voltage to 0.4V. The low voltage feature from FBB leads to 34% power dissipation reduction to 4.7mW. The power gain ($S_{21}$) > 7dB and noise figure < 4.1 dB can be achieved over the bandwidth of 3.1–8.2GHz. Good linearity is presented with IIP3 as high as 2dBm and 6dBm at 4GHz and 10GHz, respectively. The chip size is as small as 0.388mm$^2$, even with an extensive use of inductors in LC-ladder filter and inductive peaking circuit for bandwidth extension.

I. Introduction

UWB LNA is as a key component for wideband transceiver with target bandwidth in 3.1–10.6 GHz. Among the existing solutions for wideband amplifiers design, distributed amplifier (DA) was widely used, due to its intrinsic broadband response with good input and output impedance matching. However, high power consumption and large chip area becomes a roadblock hampering its applications in widespread system [1-3]. Recently, RC feedback topology becomes increasingly popular attributed to the advantage of superior broadband matching and flat gain. Unfortunately, it cannot offer sufficient gain and lower noise figure (NF) under the criterion of low power consumption [4-5]. Common gate topology [6] is one more potential solution to approach broadband input matching, but the mentioned weaknesses and trade-offs in gain, noise, and power dissipation remains a critical problem. For UWB technology to be viable in the hand-held wireless applications, low power dissipation brings the toughest challenge. In this paper, a UWB LNA was proposed and implemented using 130 nm 1.2V CMOS process to attain the goal of broadband impedance matching, low noise figure (NF), low voltage and low power consumption, and small chip area.

II. UWB LNA Circuit Design and Analysis

Fig.1 illustrates the circuit schematics of the proposed UWB LNA, which is composed of LC-ladder filters for input matching stage, cascode for amplifying stage, inductive peaking circuit for bandwidth extension, and source follower for output buffer stage. First, for the input matching stage, a 3-section LC-ladder filter, namely Chebyshev filter was adopted, combining $C_{gs}$ of M1 and source degeneration inductance $L_{D}$ to realize broadband matching. Secondly, for the amplifying stage, a cascode topology with forward body biasing (FBB) scheme was implemented to reduce $V_{DD}$ and power consumption. The cascode amplifier can offer the advantages, such as less Miller effect, better reverse isolation, wider frequency response, and lower noise figure [7-8]. Inductive peaking method can improve the power gain at higher frequency and extend the usable bandwidth. Finally, for the source follower buffer stage, an output matching buffer composed of M3, L3, and C3 shown in Fig.1 was designed to improve the gain at high frequency and achieve flat gain over the entire bandwidth. According to the schematics and small signal equivalent circuit of an inductive peaking amplifier shown in Fig. 2(a) and (b), the transfer function $H(s)$ without and with $L_d$ can be expressed by (1) and (2). Fig. 3 demonstrates the inductive peaking effect from $L_d$ on the UWB LNA performance, such as power gain ($S_{21}$), noise figure (NF), input return loss ($S_{11}$), and output return loss ($S_{22}$), calculated by ADS simulation. Note that the inductive peaking circuit adopting $L_d$ can effectively improve the UWB performance to higher $S_{21}$ and lower NF.

$$H(s) = \frac{g_m (R_g) / s C_{out}}{s C_{out} + 1} = \frac{1}{s R_g C_{out} + 1}$$

$$H(s) = \frac{g_m (R_g + s L_d) / s C_{out}}{s C_{out} + 1} = \frac{1}{s R_g C_{out} + s L_d R_g + 1}$$

The cascode topology has been widely used in amplifier like LNA but the stacked transistors structure demands higher $V_{DD}$ to ensure that M2 can operate in saturation region. According to body biases, the adoption of FBB can facilitate $V_T$ and $V_{DD}$ scaling. The FBB effect on the proposed UWB LNA performance was verified by ADS simulation. The results shown in Fig. 4 indicates that FBB ($V_{BS} = 0.4V$) can significantly enhance LNA performance under very low voltage ($V_{DD} = 0.9V$, $V_{GS} = 0.4V$), such as higher gain ($S_{21}$), lower noise figure (NF), and lower return loss at both input and output nodes ($S_{11}$ and $S_{22}$).

II. Results and Discussion

Fig. 5 illustrates the chip micrograph and on-wafer measurement setup. The chip area is as small as 0.388mm$^2$. The equipment configuration includes a microwave network analyzer (Agilent PNA-X N5242A) for S-parameters and linearity measurement, a spectrum analyzer (Agilent E4448A) with an option for NF analysis, and dc power supplies for $V_{DD}$ and $V_{GS}$. Fig. 6 presents the performance measured from the UWB LNA, in a wide bandwidth. As shown in Fig. 6(a), the power gain $S_{21} > 7$ dB and reverse isolation $S_{11} < -27.3$ dB have been achieved over the bandwidth of 3.1–8.2GHz and the maximum $S_{21}$ can reach 10.8 dB. The NF shown in Fig. 6(b) can be maintained below 4.1 dB within the mentioned bandwidth and match very well the prediction from post-simulation. The wideband input and output matching is proven by sufficiently low $S_{11}$ and $S_{22}$, illustrated in Fig. 6(c). Furthermore, Fig. 6(d) indicates stability $\mu > 1$ over the wideband and ensures the immunity from abnormal oscillation. Regarding the linearity of major concern for sufficient dynamic range under low voltage operation, the input referred third order intermodulation intercept point, namely IIP3 was determined by two tones measurement. Fig. 7(a) and (b) demonstrate the output power ($P_{out}$) versus input power ($P_{in}$) measured at two different frequencies, in which the fundamental and third-order intermodulation (IMD3) components were presented for the determination of IIP3. The results indicate promisingly good linearity with IIP3 as high as 2 dBm and 6 dBm at 4GHz and 10GHz, respectively. The increased IIP3 at higher frequency suggests a trade-off between the power gain ($S_{21}$) and linearity (IIP3). Note that all of the presented performance for this UWB LNA was measured under $V_{DD} = 0.9V$, $V_{GS} = 0.4V$, and $V_{BE} = 0.4V$ for FBB. The extremely low voltage operation enabled by FBB leads to 34% power dissipation reduction to 4.7 mW.

Table I summarizes UWB LNA performance in recent publications [9-12] and this work from our design based on state-of-the-art technologies. The comparison indicates that the UWB CMOS LNA realized in this work offers the advantages of lower $V_{DD}$, lower power consumption, higher linearity (IIP3), and...
smaller chip size. According to the figure-of-merit (FOM) defined by (3), including $S_{21}$, bandwidth (BW), noise factor (F), power dissipation ($P_{dd}$), and IIP3, our proposed UWB LNA can achieve the best record in terms of FOM and FOM/chip size, with major contribution from lower $P_{dd}$ and higher IIP3.

$$FOM = \frac{S_{21} \times BW}{(F-1) \times P_{dd}}$$

(3)

### Table I UWB LNA Performance Benchmark

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<tr>
<th>Technology</th>
<th>This work</th>
<th>[9]</th>
<th>[10]</th>
<th>[11]</th>
<th>[12]</th>
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<td>BW (GHz)</td>
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<td>3.1~10.6</td>
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<tr>
<th>$I_{IP3}$ (dB)</th>
<th>9~12</th>
<th>9.2~10</th>
<th>7.3~9.2</th>
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<td>&lt; -9.7</td>
<td>&lt; -11.2</td>
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<td>$S_{21}$ (dB)</td>
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<td>&lt; 18.5</td>
<td>&lt; 14</td>
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<tr>
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<table>
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<th>Topology</th>
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<th>2-stage Transformer feedback</th>
<th>Cascade FBB LC filter</th>
<th>CMOS Dual feedback</th>
<th>2-stage CE Resistive feedback</th>
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### Acknowledgement

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### References


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Fig. 1 The circuit schematics of UWB LNA consisting of an input matching network, cascade amplifier, inductive peaking circuit, and an output buffer.

Fig. 2 (a) The schematics of an inductive peaking amplifier (b) small signal equivalent circuit for inductive peaking analysis.

Fig. 3 The inductive peaking effect from $L_4$ effect on UWB LNA performance from ADS simulation (a) $S_{11}$ (b) $S_{21}$ (c) $S_{12}$ (d) $S_{22}$.

Fig. 4 Comparison of UWB LNA performance under ZBB and FBB simulated by ADS (a) $S_{11}$ (b) NF (c) $S_{11}$ (d) $S_{22}$.

Fig. 5 On-wafer measurement setup for UWB LNA chip characterization.

Fig. 6 UWB LNA performance measured under $V_{DD}$=0.9V and $V_G$=0.4V (FBB) and over a wide band of frequencies $1$~$12$GHz (a) $S_{11}$ (b) $S_{11}$ (c) $S_{12}$ (d) stability factor $\mu$.

Fig. 7 Linearity $P_{out}$ vs. $P_{in}$ measured from UWB LNA under $V_{DD}$=0.9V, $V_G$=0.4V (FBB) (a) $I_{IP3}$=2dBm at 4GHz (b) $I_{IP3}$=6dBm at 10GHz.