Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1039-1040

In-pixel type small-scale integrated C-V converter with chopper stabilized CMOS inverter

Ryo Kodama[1], Hajime Miyao[1], Makoto Ishida[1] and Hidekuni Takao[1, 2]

[1] Toyohashi University of Technology, Dept. Electrical and Electronic Engineering
1-1 Hibarigaoka, Tempaku, Toyohashi, Aichi, 441-8580, Japan.
[2] Kagawa University, Micro-Nano Structure Device Integrated Research Center
2217-20, Hayashi, Takamatsu, Kagawa, 761-0396, Japan.
Phone: +81-87-864-2331 E-mail: takao@eng.kagawa-u.ac.jp

1. Introduction

Recently, MEMS microsensor devices with integrated array of capacitance sensor elements have been important in various applications. Fig. 1 shows a conceptual diagram of highly sensitive micro-force sensor array with integrated array of capacitive sensors [1, 2]. The pixel structures are fabricated by post-CMOS integration technology of MEMS, and C-V converter circuit is necessary to be integrated in each pixel since the capacitance change is very small as compared to stray capacitance. Although C-V converter with operational amplifiers realizes a high performance, it requires high voltage for power supply, consumes a large power, and occupies a large area in a pixel. Therefore, small-scale C-V converter circuit is essential to integrate it in each pixel circuit for realization of fine-pitch pixel array and small power consumption. In this paper, a small-scale, in-pixel type C-V converter with chopper stabilized CMOS inverter is newly proposed and reported for arrayed MEMS capacitive sensors. The small-sized capacitive sensor for sensor array is buried in the stray capacitor as wiring capacitors and FET-gate capacitors. Reduction and cut-down of a stray capacitance is very important for small capacitance detection below 1pF. The wiring capacitors around the sensor are cut-downed by in-pixel type detection circuit. C-V converter with operational amplifier can minimize stray capacitance effect by means of the fixed potential of inverting input terminal with negative feedback effect. In the new C-V converter of this study, clocked chopper stabilized CMOS inverter [3] is used instead of large-scale operational amplifiers to realize negative feedback circuit scheme for stray capacitance reduction.

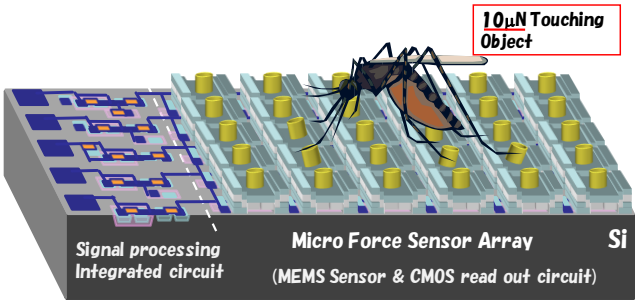


Fig.1. Highly sensitive micro force sensor array [1, 2]

2. C-V conversion circuits in the pixel

C-V conversion circuits

Fig. 2 shows a schematic diagram of the C-V converter circuit with a chopper stabilized CMOS inverter. The operating point of the inverter is set in its high-gain region by dynamic biasing with switched capacitor. The bias point is kept by the sensor capacitor (C_{sense}) as temporary stored charge. Applying a pulse voltage to the sensor capacitor, the capacitance is converted into a voltage swing of the inverter output due to charge transfer. Detail of the circuit operation is as following.

(a) Reset operation phase

In the reset phase, the inverter is biased to its transition region to get higher open-loop gain. M1 is turned on by the reset signal to short the inverter input and output, and M2 is also "ON" to discharge C_{sense}. Contrary, M3 is turned off. In this case, the circuit is operating as shown in Fig. 3 (a). Charge in each capacitor and input/output voltage in the inverter are calculated as eq. (1) where V_{gnd} is 0V, and V_{offset} is the offset voltage of the CMOS inverter.

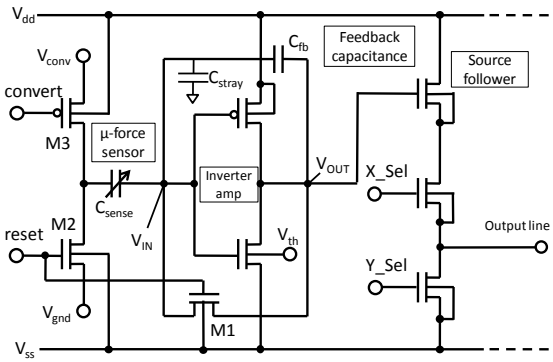
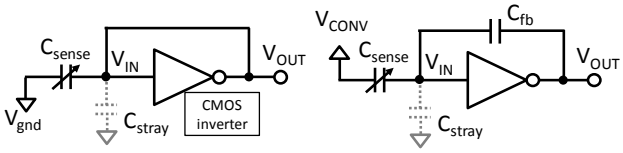


Fig.2 Schematics of the micro-force sensor pixel



(a) Reset operation (b) C-V conversion operation

Fig.3 Operation of the C-V conversion circuits

$$\begin{cases} V_{IN} = V_{OUT} = V_{offset} \\ Q_{sense} = C_{sense} \times (V_{offset} - 0) \\ Q_{fb} = C_{fb} \times (V_{IN} - V_{OUT}) = 0 \\ Q_{stray} = C_{stray} \times (V_{offset} - 0) \end{cases} \quad (1)$$

(b) C-V conversion phase

In the C-V conversion phase, M1 and M2 are turned off to keep the inverter in operation mode, and then, M3 is turned on to drive the electrode of C_{sense} from V_{gnd} to V_{conv}. In this case, the circuit is operating as shown in Fig. 3 (b). Charge of C_{sense} corresponding to the pulse voltage is transferred to C_{fb}. Charge in each capacitor and the output voltage is expressed as eq. (2), where A is the open-loop gain of the dynamically biased chopper-inverter.

$$\begin{cases} V_{OUT} = -A \times V_{IN} \\ Q_{sense}' = C_{sense}(V_{offset} + V_{IN} - V_{conv}) \\ Q_{fb}' = C_{fb}(V_{offset} - V_{OUT} - V_{offset} - V_{IN}) \\ Q_{stray}' = C_{stray}(V_{offset} + V_{IN} - 0) \end{cases} \quad (2)$$

Because charge and discharge in eqs. (1) and (2) are the transfer on the floating node (V_{in}), total electric charge is expressed as eq. (3).

$$Q_{sense} + Q_{fb} + Q_{stray} = Q_{sense}' + Q_{fb}' + Q_{stray}' \quad (3)$$

V_{out} can be derived from eqs. (1), (2) and (3) as eq. (4).

$$V_{\mathrm{out}} = \frac{\dfrac{-A}{(1+A)}}{1 + \dfrac{C_{sense}}{(1+A)C_{\mathrm{fb}}} + \dfrac{C_{\mathrm{stray}}}{(1+A)C_{\mathrm{fb}}}} \cdot \frac{C_{\mathrm{sense}}}{C_{\mathrm{fb}}} V_{conv} \quad (4)$$

The analytical eq. (4) shows the output voltage swing of the C-V converter. According to eq. (4), the effect of stray capacitance is much reduced to 1/(1+A). Sensitivity instability due to stray capacitance is much reduced by the negative feedback effect. Combining the correlated double sampling (CDS) technique, offset instability is also eliminated.

Fig.4 shows a comparison of eq. (4) and a result of SPICE simulation. The C-V conversion gain is estimated as 20mV/fF. The parameters used for the estimation is as following; open-loop gain of the chopper inverter is 36.9dB, C_{fb} is 49fF, C_{stray} is 500fF, and V_{CONV} is 1.2V. The two results are corresponding very well. Therefore, the operation principle of the new C-V converter has been confirmed and designed for fabrication of the prototype.

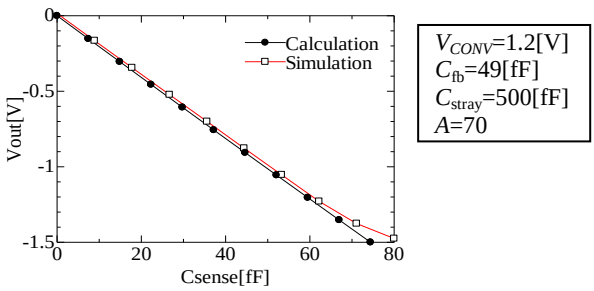


Fig.4. SPICE simulation of C-V converter

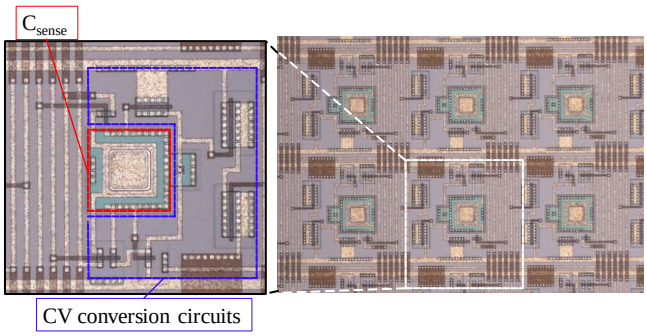
Fabrication and Evaluation of C-V conversion circuits

Fig. 5 shows microscopic images of a fabricated device. The C-V converter is integrated with capacitive micro-force sensor device. The size of capacitive sensor pixel is 380×380μm^2. The C-V conversion circuit is integrated around the capacitive micro force sensor structure fabricated by post-CMOS micromachining.

The conversion performance of the C-V converter was evaluated. In order to evaluate the negative feedback effect of CMOS inverter amplifier, the C-V conversion characteristic is compared with that of "passive C-V converter" without inverter amplifier [1, 2] as shown in Fig. 6. If there is no stray capacitance in the circuit, the theoretical conversion gain of the each C-V converter is expected to be 49.5mV/fF. In Fig. 6, the conversion gain of the passive C-V converter is degraded to 2.8mV/fF due to the stray capacitance. On the other hand, the new C-V converter with CMOS inverter shows 18.4mV/fF conversion gain. This result clearly shows that performance degradation of C-V converter due to stray capacitance effect is effectively reduced to 1/6 by only using the very simple CMOS inverter.

3. Conclusions

In this paper, a small-scale, in-pixel type C-V converter with chopper stabilized CMOS inverter has been proposed and demonstrated for MEMS capacitive sensor array. The new C-V converter realizes a higher conversion gain and lower stray capacitance sensitivity with a small size and simple CMOS inverter amplifier.



(a)Pixel (b)Array

Fig.5 Fabricated devices of the sensor pixel

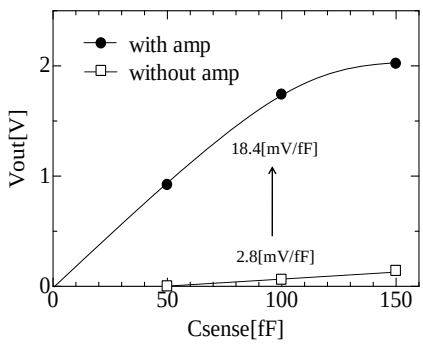


Fig. 6 C-V conversion performance

References

[1]R. Kodama, H. Takao, et al, *Asia-Pacific Conference on Transducers and Micro-Nano Technology* (2008).

[2]R. Kodama, H. Takao, et al, *25th Sensor symposium on Sensors, Micro machines and Application Systems*, pp.59~62 (2008).

[3] K. Kusumoto, A. Matsuzawa, et al, *IEICE Technical Report Archives*, Vol.93, No.173, pp.9~16 (1993) .